Curriculum Vitae

Personal information

Surname / First name	**Bossuet Lilian**
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Nationality	French
Date of birth	October 23, 1975, Angouleme, France.
Gender	Male

Employment

Professor at University of Saint-Etienne - CNRS
Laboratoire Hubert Curien – UMR CNRS 5518
Head of the Computer Science Department (120 members)
Head of the Embedded System Security Group (17 members)

Teaching at Telecom Saint-Etienne (member of French Institute of Telecom)

Current Position

Working experience

2000 - 2001	Teaching Assistant at the University of Rennes, France
2001 – 2004	Ph.D. Student, Research and Teaching Assistant at the University of South Brittany, Lorient, France
Summer 2003	Visiting Researcher at the University of Massachusetts, Amherst, USA
2004 – 2005	Assistant Professor at the University of South Brittany, Lorient, France
Summer 2005	Invited Researcher at the University of Massachusetts, Amherst, USA
2005 -2010	Associate Professor at the Bordeaux Institute of Technology, France
2008 -2010	Head of the Embedded System Department at the Bordeaux Institute of Technology, France
2010 -2017	Associate Professor at the University of Saint-Etienne, France

Education and training

1999	Bachelor of Science in Electrical Engineering Ecole Nationale Supérieure de l'Electronique et de Ses Applications, Cergy-Pontoise, France
2000	Electrical Engineering Competitive Examination for Teacher Training Ecole Normale Supérieure de Cachan, France
2001	Master of Science in Electrical Engineering Institut National Supérieur des Sciences Appliquées – University of Rennes, France
2004	Ph. D. in Electrical Engineering University of South Britanny, Lorient, France
2010	Accreditation to Supervise Research in Electrical Engineering (French *Habilitation à Diriger des Recherches*) University of Bordeaux, France

Personal skills and competences

My research is in the general area of embedded systems design, including hardware security of embedded systems (data, intellectual property and system security) and reconfigurable hardware design.

Active research topics	Hardware security, war against illegal IC copy and counterfeiting, IP protection, PUF design and characterization, side channel attacks and countermeasures, TRNG attack, MCryptoPSoC architecture and design, crypto-processor architecture and design, embedded system security, FPGA security
Previous research topics	Reconfigurable system architecture and design, design space exploration of reconfigurable architecture, ADC design and test
Teaching topics	Hardware security, applied cryptography, digital system design, digital signal processing, embedded system design and application, FPGA architecture, design and application.

Publications

More than 180 scientific publications since 2002

24 papers in international journals : ACM Computing Surveys, ACM Trans. on Reconfigurable Technology and Systems, IEEE Trans. on Forensic and Security, IEEE Trans. on VLSI, IEEE Trans. on Computer Aided Design, IEEE Trans. on Instrumentation and Measurement, IEEE Embed. Sys. Letter, Springer Design Automation for Embedded System, WHILEY Intern. J. of Circuit Theory and App., ELSEVIER MICPRO, IET Comp. and Digit. Techn., Shaker-Verlag Trans. on Syst., Sign. and Devices, EURASIP J. of Emb. Syst., Inderscience Publishers Intern. J. of Emb. Sys.

4 papers in national journals, 1 book (Springer), 11 book chapters (Springer, Kluwer, Whiley, Hermes Sciences), 15 invited talks, 1 keynote, 1 tutorial, 85 international conference papers, 16 national conference papers. H-Index :16

Advising – Ph.D. Thesis

12 Ph.D. Students (9 graduated), 5 Post-Docs, 18 M.S. Students

23 Ph.D. Thesis committees (9 as reviewer)

Research awards

Grand Prix de l'Electronique Général Ferrié (2016)

French Outstanding research award (PEDR 2006/2010 - PES 2010/2016 - PEDR 2016/2020)

IEEE Senior Member (since 2015)

Outstanding research award – Saint-Etienne metropolis 2012

Main funding

HECTOR (2015-218) European H2020 Project, PILAS (2016-2019) FUI Project, TEEVA (2015-2018) FUI Project, SALWARE (2013-2017) French ANR JCJC Project, TSUNAMY (2013-2017) French ANR INS Project, EMAISeCi (2010-2014) French ANR ARPEGE Project, SCALA (2010-2013) French Institute of Telecom Project, SecReSoC (2009-2013) French ANR ARPEGE Project, LIFEMIT (2008-2011) French ANR PREDIT Project, ERGAP (2010-2012) DGA Research Project.

Industrial grants: STMicroelectronics, GEMALTO, DGA, NXP, SAFT, Orange Lab.

Institutional responsibilities

Elected member of the Board of Directors of the Jean Monnet University (20 000 students, 5 faculties, 4 institutes) (2015-2017)

Member of Scientific Committees: ENSEIRB (2009-2010), Univ. of South Britany (2001-2003)

EE Graduate Curriculum Committees: Telecom Saint-Etienne (head, 2010-present), MASTER EEAP INSA Lyon (2010-present), ENSEIRB (2005-2010)

Recruitment Committees of Associated Professor (Evaluator): Univ. of South Britany (2014, 2011 and 2010), Grenoble Institute of Tech. (2014), Bordeaux Institute of Tech. (2012 and 2011), Univ. of Montpellier (2012), Univ. of Saint-Etienne (2011), Univ. of Bordeaux (2010, 2009, 2008 and 2007).

Professional service

Guest Editor Special Issue on Trustworthy Manufacturing and Utilization of Secure Devices, ELSEVIER Microprocessors end Microsystems 2016

Organization committee member of international conferences: ReCoSoC, CryptArchi, TRUDEVICE Workhsop and summer school

Organization of special sessions: NEWCAS'11, ReCoSoC'11, IEEE SCS'09, IEEE ICECS'06

Review committee member of international journals: IEEE Transactions on Computer, IEEE Trans. on Information Theory, ACM Trans. on Reconfigurable Technology and Systems, ACM Trans. on Embedded Computing Systems, EURASIP Journal of Embedded System

Review committee member of international conferences: DATE'16, CHES'16, DATE'14, DATE'13, DATE'12, DASIP'12, ReCoSoC'12, COSADE'12, ISSPA'12, ICCCT'12, ReConFig'12, ReCoSoC'11, NEWCAS'11, ReConFig'10, CHES'10, ARC'10, NEWCAS'10, SCS'09, DASIP'09, CryptArchi'09, CHESS'09, NEWCAS'09, ISCAS'09, ISVLSI'08, ICECS'08, ICECS'07, JNRDM'07, PRIME'07, DASIP'07, ICECS'06, DCIS'06, ERSA'06, ERSA'05, FPL'03, RAW'03

Review committee member of international book editor: Wiley and Sons

Review committee member for research programs: ANR Systèmes embarqués et grandes infrastructures, ANR Jeunes Chercheurs, ANR Emergence, ANR Blanc

Member of scientific networks and societies

Member of the French CNRS scientific network on System-On-Chip and System-in-Package (GDR SoC-SiP). Member of Board of Directors and Strategy Committee, Leader of the Working Group on Trusted Hardware (one of the four working groups of this national network).

Member of the European scientific network of excellence on Trustworthy Manufacturing of Secure Devices EU-COST action IC1204 TRUDEVICE. Leader of the Working Group on Trustworthy Manufacturing of Secure Devices (one of the five working groups of this EU cost action).

IEEE Senior Member (M 2010, SM 2015); ACM Member (since 2015), CryptArchi Senior Member.