## Arithmetic Operators for Pairing-Based Cryptography

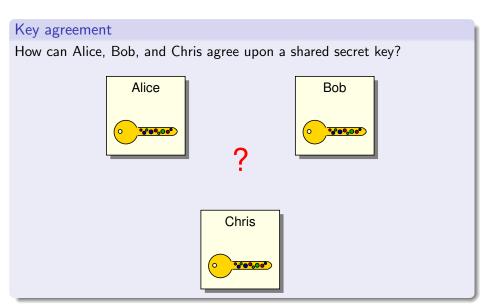
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#### Outline of the Talk

- 1 Example: Three-Party Key Agreement
- 2 Computation of the  $\eta_T$  Pairing
- 3 A Coprocessor for the Full Pairing Computation
- 4 Conclusion



### Discrete logarithm problem (DLP)

- $G = \langle P \rangle$ : additively-written group of order n
- DLP: given P, Q, find the integer  $x \in \{0, \dots, n-1\}$  such that Q = xP

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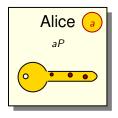
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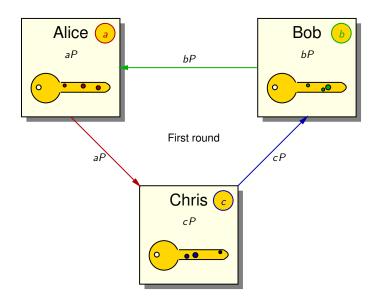








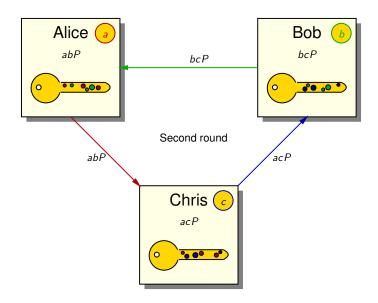


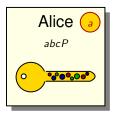




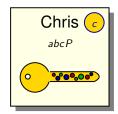












Three-party two-round key agreement protocol

Does a three-party one-round key agreement protocol exist?

### Bilinear pairing

- $G_1 = \langle P \rangle$ : additively-written group
- G2: multiplicatively-written group with identity 1
- A bilinear pairing on  $(G_1, G_2)$  is a map

$$\hat{e}:\textit{G}_{1}\times\textit{G}_{1}\rightarrow\textit{G}_{2}$$

that satisfies the following conditions:

**1 Bilinearity.** For all Q, R,  $S \in G_1$ ,

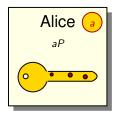
$$\hat{e}(Q + R, S) = \hat{e}(Q, S)\hat{e}(R, S)$$
 and  $\hat{e}(Q, R + S) = \hat{e}(Q, R)\hat{e}(Q, S)$ .

- **2** Non-degeneracy.  $\hat{e}(P, P) \neq 1$ .
- Computability. ê can be efficiently computed.

Bilinear Diffie-Hellman problem (BDHP)

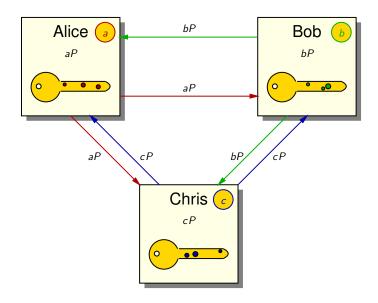
Given P, aP, bP, and cP, compute  $\hat{e}(P, P)^{abc}$ 

Assumption: the BDHP is difficult













$$\hat{e}(bP, cP)^a = \hat{e}(aP, cP)^b = \hat{e}(aP, bP)^c = \hat{e}(P, P)^{abc}$$



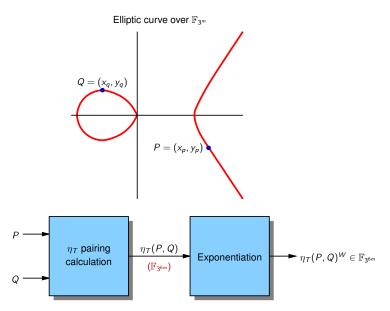
### Examples of cryptographic bilinear maps

- Weil pairing
- Tate pairing
- $\eta_T$  pairing (Barreto et al.)
- Ate pairing (Hess et al.)

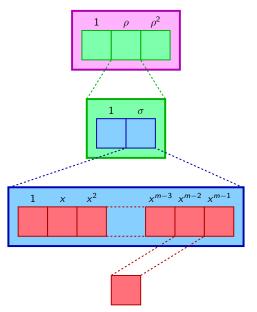
#### **Applications**

- Identity based encryption
- Short signature

## Computation of the $\eta_T$ Pairing



### Computation of the $\eta_T$ Pairing – Tower Field



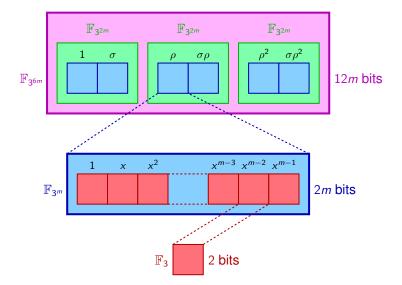
$$\mathbb{F}_{3^{6m}}=\mathbb{F}_{3^{2m}}[
ho]/(
ho^3-
ho-1)$$
  $\mathbb{F}_{3^{2m}}=\mathbb{F}_{3^m}[\sigma]/(\sigma^2+1)$ 

$$\mathbb{F}_{3^m} = \mathbb{F}_3[x]/(f(x))$$



$$\mathbb{F}_3 = \mathbb{Z}/3\mathbb{Z} = \{0, 1, 2\}$$

### Computation of the $\eta_T$ Pairing – Tower Field



# Computation of the $\eta_T$ Pairing

# $\eta_T(P,Q)$

- Addition
- Multiplication
- Cubing
- Cube root

# $\eta_T(P,Q)^{3^{\frac{m+1}{2}}}$ (Arith 18)

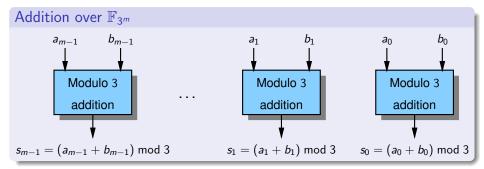
- Addition
- Multiplication
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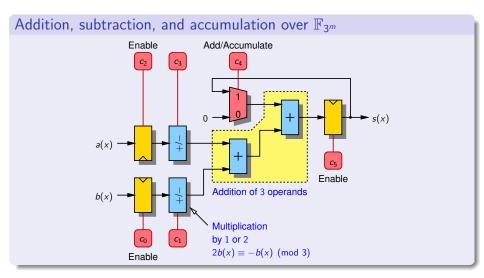
Bilinearity of 
$$\eta_T(P,Q)^W$$

$$\eta_{\mathcal{T}}(P,Q)^{W} = \sqrt[3^{m}]{\left(\eta_{\mathcal{T}}\left(\left[3^{\frac{m-1}{2}}\right]P,Q\right)^{3^{\frac{m+1}{2}}}\right)^{W}}$$

## Operations over $\mathbb{F}_{3^m}$

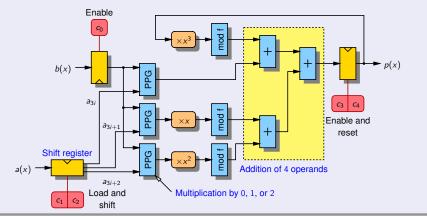
Additions	$51 \cdot \frac{m-1}{2} + 503$
Multiplications	$15\cdot\frac{m-1}{2}+86$
Cubings	10m + 2
Inversion	1

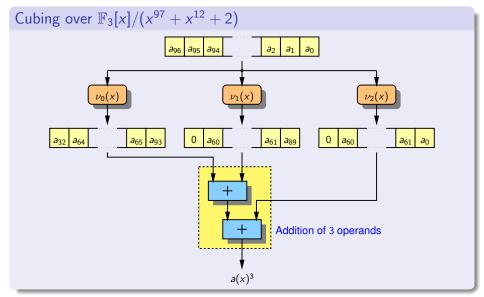




#### Multiplication over $\mathbb{F}_{3^m}$

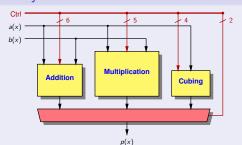
- Array multiplier ( $\lceil m/3 \rceil$  clock cycles)
- Most significant coefficient first (Horner's rule)





### Arithmetic operators over $\mathbb{F}_{3^{97}}$ on a Cyclone II FPGA

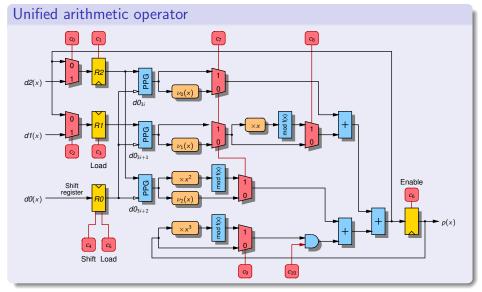
Operation	Area [LEs]	Control [bits]
Add./sub.	970	6
Mult.	1375	5
Cubing	668	4
ALU	3308	17



#### Unified arithmetic operator

- Operations
  - Addition
  - Subtraction
  - Accumulation
  - Multiplication
  - Cubing
- Area (Cyclone II): 2676 LEs (instead of 3308)
- Control bits: 11 (instead of 17)
- Inversion: Fermat's little theorem (96 cubings and 9 multiplications)

$$a^{3^m-2}=a^{-1}$$
, where  $a\in\mathbb{F}_{3^m}$ 



### Results (CHES 2007)

- FPGA: Xilinx Virtex-II Pro 4
- $\mathbb{F}_3[x]/(x^{97}+x^{12}+2)$
- Area: 1888 slices + 6 memory blocks
- Clock frequency: 147 MHz
- Clock cycles for a full pairing: 32618
- Calculation time:  $222\mu$ s

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### Extended Euclidean algorithm (EEA)

- Area: 2210 additional slices
- Clock cycles for a full pairing: 32419 instead of 32618

### Conclusion

### Comparisons

Architecture	Area	Calculation time	FPGA
Arith 18 & Waifi 2007	18000 LEs	$33\mu$ s	Cyclone II
CHES 2007	1888 slices	$222\mu \mathrm{s}$	Virtex-II Pro
Grabher and Page (CHES 2005)	4481 slices	$432\mu\mathrm{s}$	Virtex-II Pro
Kerins et al. (CHES 2005)	55616 slices	$850\mu\mathrm{s}$	Virtex-II Pro
Ronan et al. (ITNG 2007)	10000 slices	$178\mu\mathrm{s}$	Virtex-II Pro

(1 slice  $\approx$  2 LEs)

#### Conclusion

#### VHDL code generator

- Generation of an unified operator according to  $\mathbb{F}_{p^m}$  and f(x)
- Support for the following operations:
  - Addition
  - Multiplication
  - Frobenius  $(a(x)^p \mod f(x))$
  - Inverse Frobenius  $(\sqrt[p]{a(x)} \mod f(x))$

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#### Future work

- Automatic generation of the control unit
- Application (e.g. short signature)
- Genus 2
- Side-channel



