

# Protecting communications in bus-based MPSoCs using hardware firewalls

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## Abstract

The need for security in embedded systems has strongly increased since several years. Nowadays, it is possible to integrate several processors in a single chip. The design of such multiprocessor systems-on-chip (MPSoC) must be done with a lot of care as the execution of applications may lead to potential vulnerabilities such as revelation of critical data and private information. Among the critical points, protection of the communications is very sensible as most of the data are exchanged through the communication architecture of the system.

This paper targets this point and proposes an efficient (in terms of latency-area trade-off) and distributed solution based on full hardware interfaces to protect AXI-based MPSoC architectures. This solution does not require software modifications and should be portable to other technologies using ARM communication standard. A case study implemented on Virtex-6 FPGAs is given in this work. The reliability of our solution is studied on larger-scale architectures using a set of benchmarks and a comparison with existing solutions.