

Embedded OS for FPGA platform: a Hardware-to-Software Security Overview

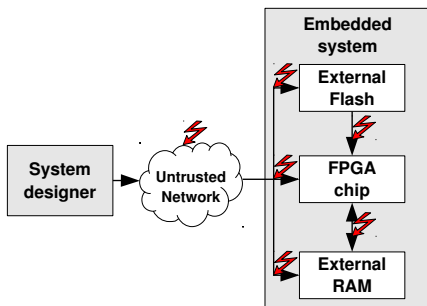
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² SAS NETHEOS, Montpellier, France

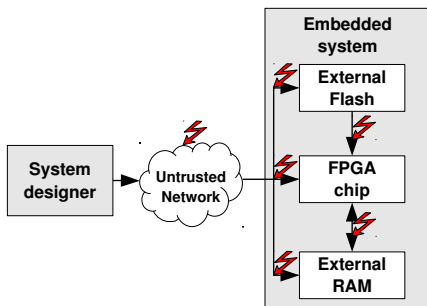
June 16, 2011





Goals

- Secure the **bitstream**, the **boot** and finally the **execution** of an embedded OS (stored in an external memory) on FPGA.
- **Upgraded** the system through an insecure network.
- Prevents an attacker to execute his own potentially **malicious program** or to **replay** an old bitstream to downgrade the system.



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→ **Man in the middle, off-chip probing and injections**

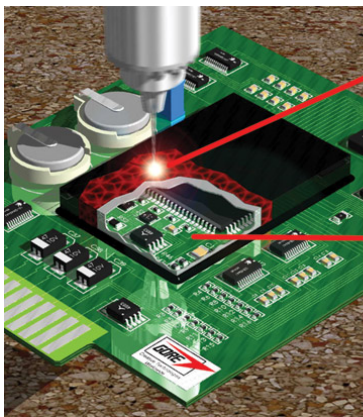
Outline

- 1 Securing the bitstream
- 2 Securing the kernel boot
- 3 Securing the Run-Time
- 4 Conclusion and future works

Outline

- 1 **Securing the bitstream**
 - FPGA chip
 - Bitstream confidentiality and integrity
 - Secure update principle
- 2 Securing the kernel boot
- 3 Securing the Run-Time
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FPGA chip

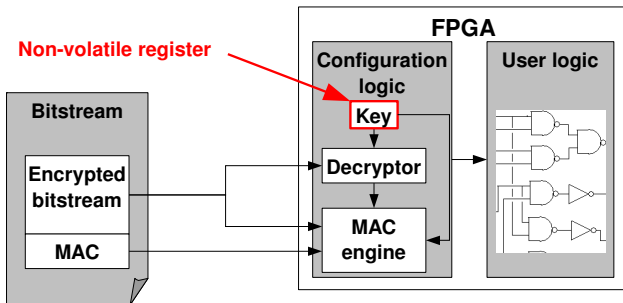


GORE™ Tamper Respondent Surface Enclosure detects physical penetration attempt and triggers module to erase sensitive information

Components requiring protection

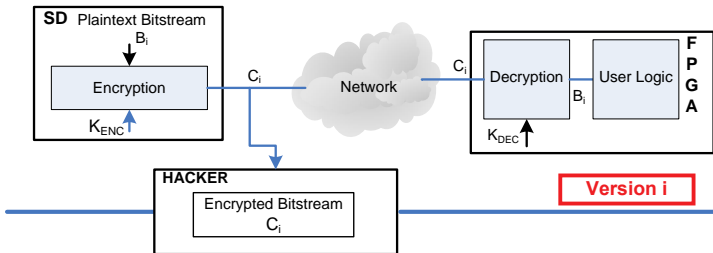
more information on <http://www.gore.com/en-xx/products/electronic/anti-tamper/tamper-surface-enclosure.html>

Bitstream confidentiality and integrity

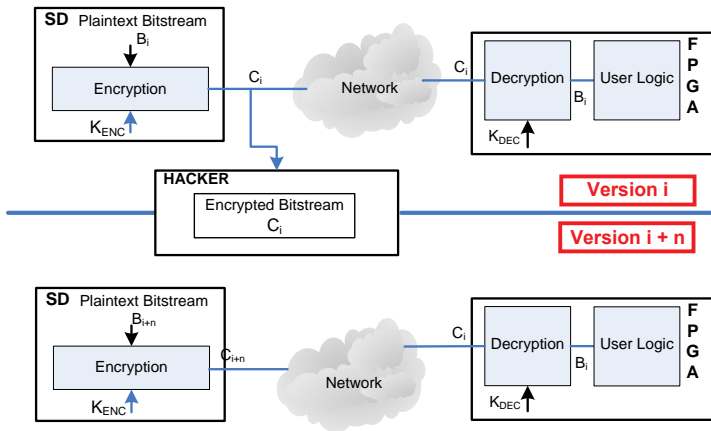


- Prevent cloning
- Prevent reverse engineering
- Prevent modifications

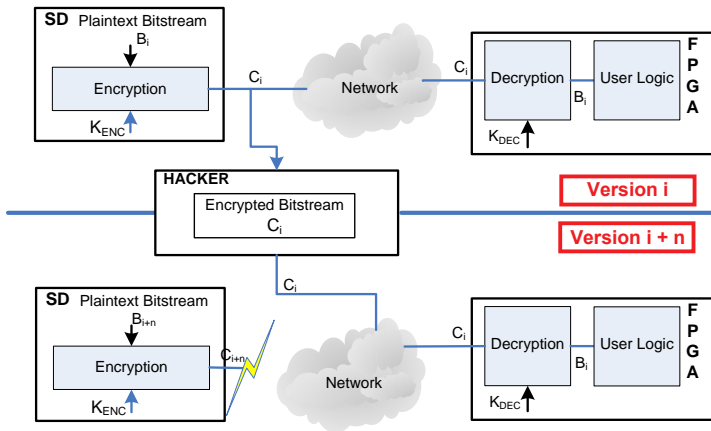
Replay attack



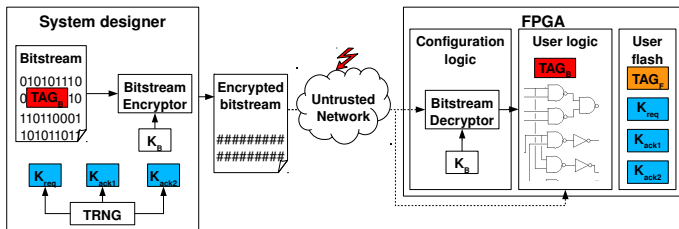
Replay attack



Replay attack



Principle with an embedded Flash



Goal : Lock the FPGA to a dedicated version

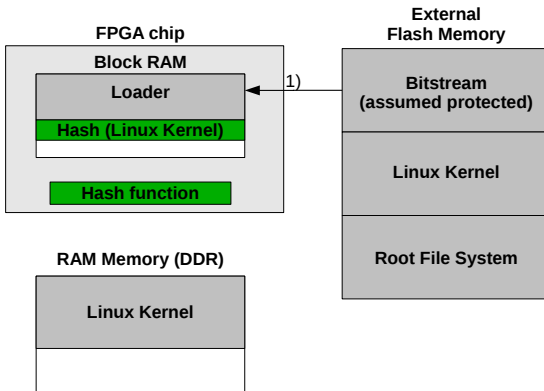
TAG_B and TAG_F are the current bitstream version

- K_{req} : for the Update command
- K_{ack1} : for the Update command acknowledgement
- K_{ack2} : for the new bitstream version startup acknowledgement

Outline

- 1 Securing the bitstream
- 2 **Securing the kernel boot**
 - Boot integrity verification
 - Using Asymmetric cryptography to add flexibility
- 3 Securing the Run-Time
- 4 Conclusion and future works

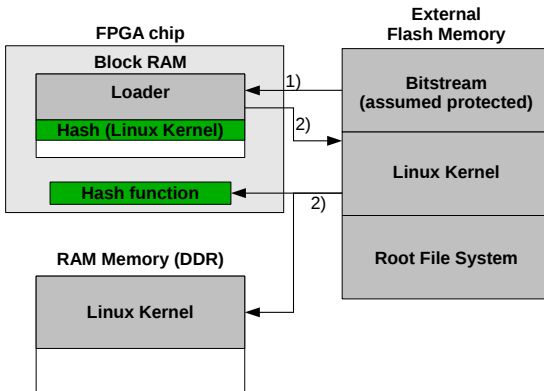
Integrity verification



Boot steps :

- 1) The loader is stored in block RAM at power-up from bitstream
- 2) The loader copies Kernel from Flash to RAM and compute its hash
- 3) The loader verifies the Kernel integrity thanks to the hash
- 4) The loader branches to the Kernel and Linux boots

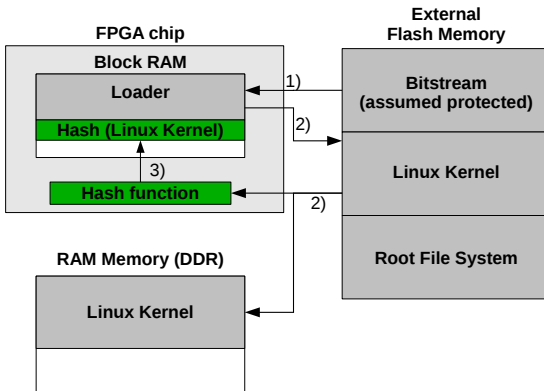
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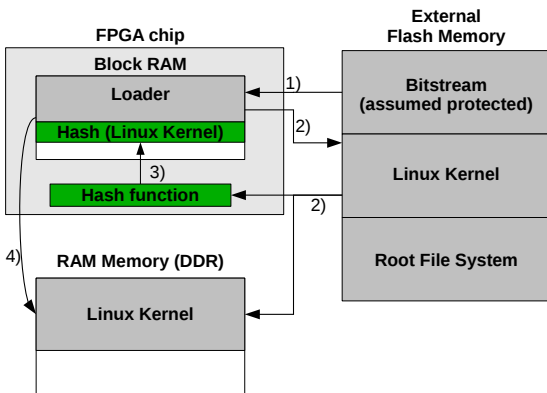
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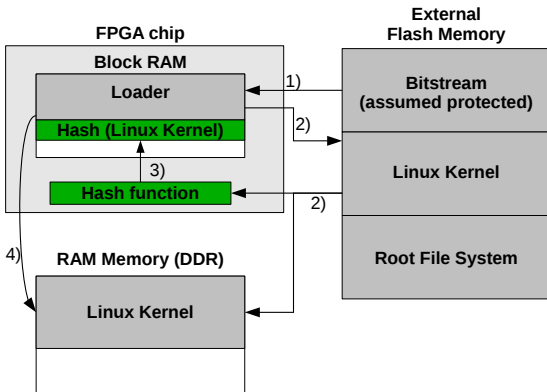
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→ **Changing the kernel requires to change the bitstream**

Performance overhead

Results :

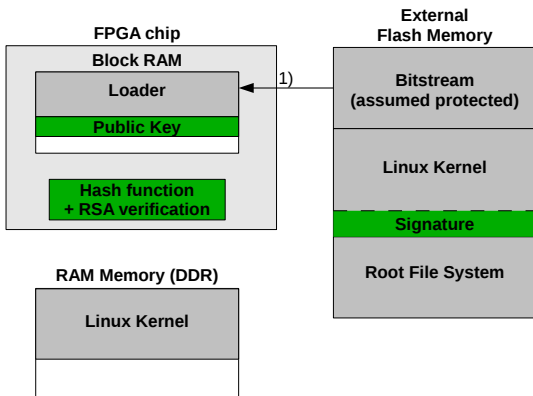
Linux kernel = 2.8 MB

Virtex 6 : Processor frequency = 100Mhz

Hash algorithm = Sha-256

IP	# Cycles	Boot time Overhead	Throughput	Gain
Soft SHA-256	295 860 775	2,959 s	0,95 MB/s	ref.
Hard SHA-256	38 376 545	0,384 s	7,29 MB/s	x7,7
+ DMA transfer	4 221 304	0,042 s	66,67 MB/s	x70

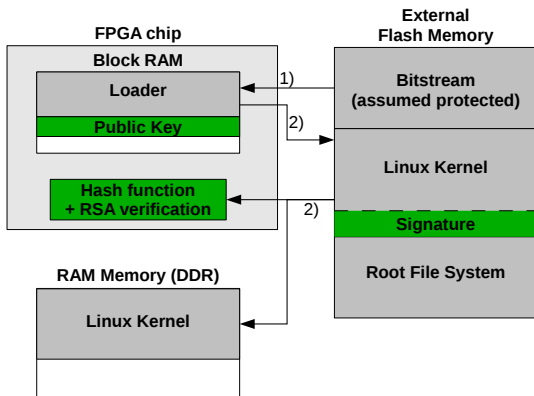
Adding flexibility



Boot steps :

- 1) The loader is stored in block RAM at power-up from bitstream
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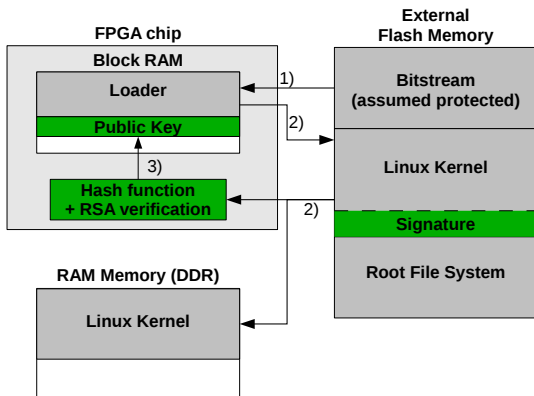
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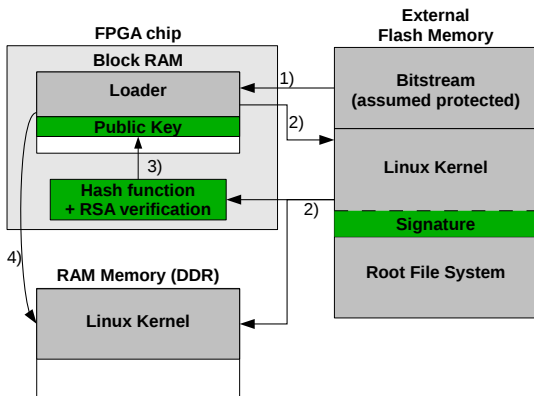
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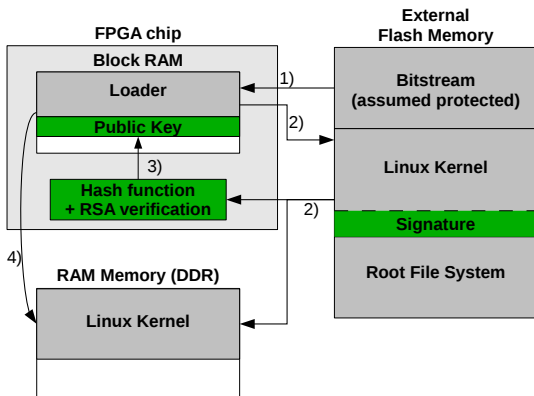
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→ This flexibility makes the kernel vulnerable to replay attacks

Security concerns

IP	# Cycles	Boot time Overhead	Throughput	Gain
RSA-1024	92 867	0,001 s	N/A	N/A

Discussion

- This flexibility makes the kernel **vulnerable to replay** attacks.
- In case of **critical security update** of the kernel, it is possible to **regenerate an asymmetric key-pair** and update the bitstream.
- *Possibility to store the key-pair in the user non-volatile memory : kernel protected against replay attacks without change the bitstream.*

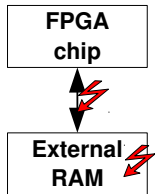
Area overhead

		Details			Total				
Strategies	Components	Slice FF	Slice LUT	BRAM	Slice FF	Slice LUT	BRAM	Fraction of V6 VLX240T	
Base system (or with soft SHA-256)	Microblaze	3 196	3 874	19					
	Cache	6	14	16					
	DDR3	5 091	4 245	11					
	Flash PLB	479 178	389 657		8 950	9 179	46	6% + 11% de BRAM	
+ Hard SHA-256	SHA (+wrapper) Interrupt ctrl.	1 509 190	1 897 180	1	10 649	11 256	47	7% + 11% de BRAM	+1%
+ DMA	Central DMA	561	799		11 210	12 055	47	8% + 11% de BRAM	+1%
+ RSA-1024	RSA (+wrapper)	684	989	4	11 894	13 044	51	9% + 12% de BRAM	+1%

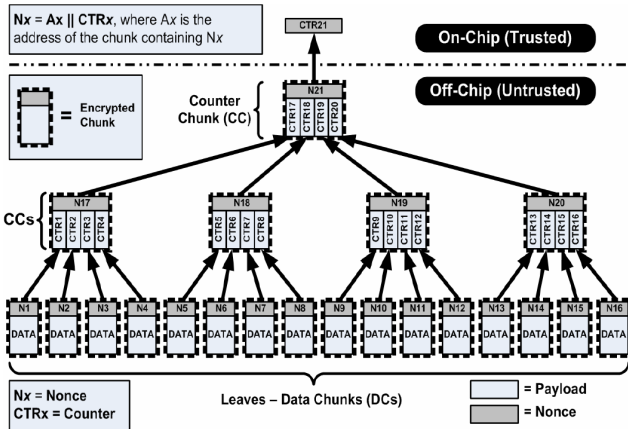
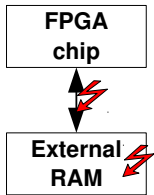
Outline

- 1 Securing the bitstream
- 2 Securing the kernel boot
- 3 Securing the Run-Time**
 - RAM protection
 - Resources isolation
 - TPM
 - Sandboxing
 - Virtualization
- 4 Conclusion and future works

RAM protection : Merkle-tree

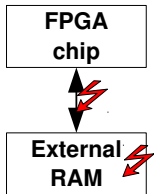


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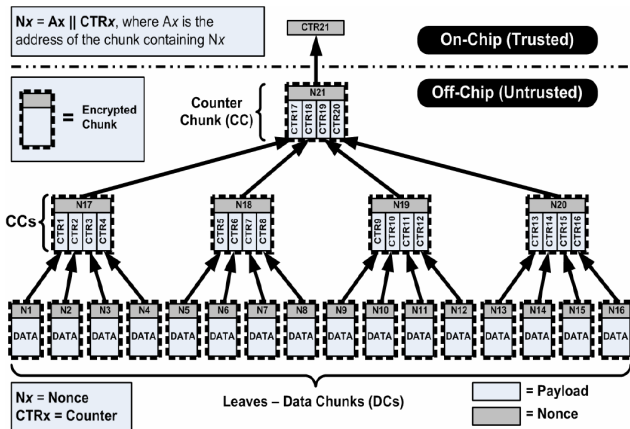


R. Elbaz, D. Champagne, R. Lee and L. Torres, "TEC-Tree : A Low-Cost, Parallelizable Tree for Efficient Defense Against Memory Replay Attacks" in CHES'07

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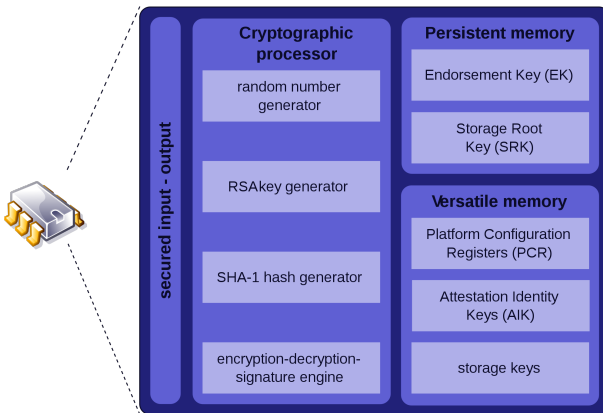


Preventing :
 replaces
 replays
 modifications
 data decryptions

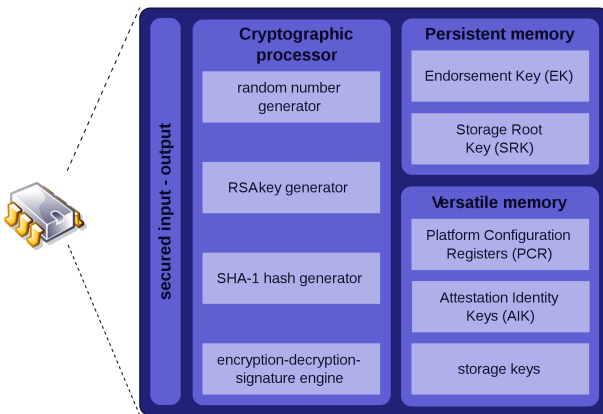


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TPM : Trusted Platform Module

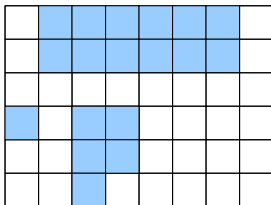


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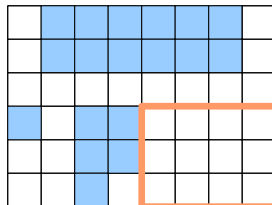


→ Can be implemented in the FPGA

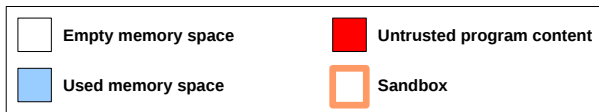
Sandboxing



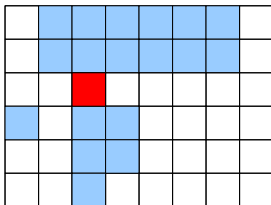
Memory (no sandbox)



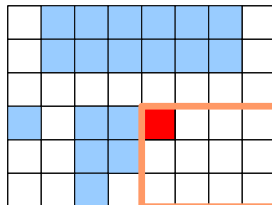
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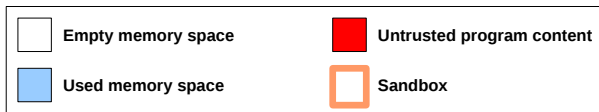
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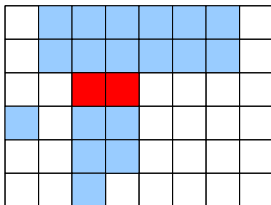
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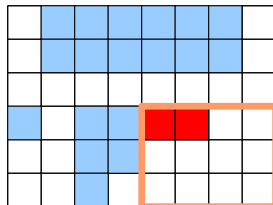
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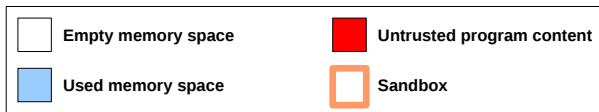
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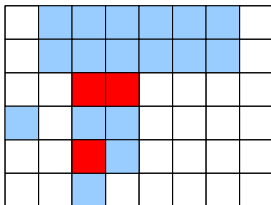
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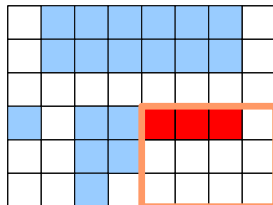
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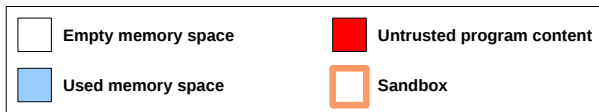
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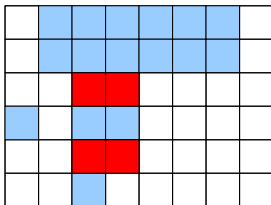
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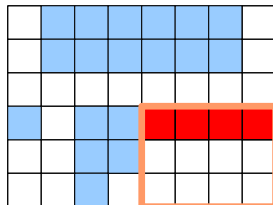
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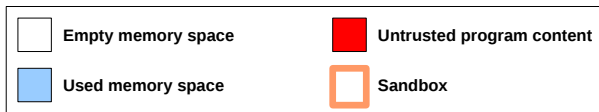
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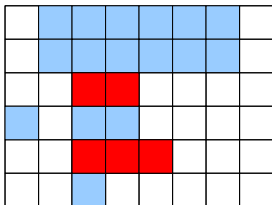
Memory (no sandbox)



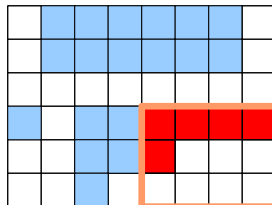
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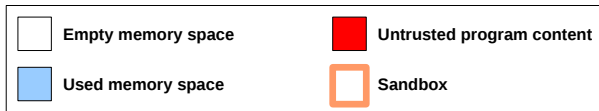
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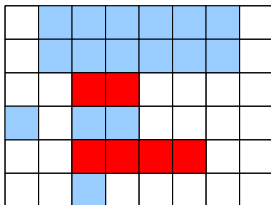
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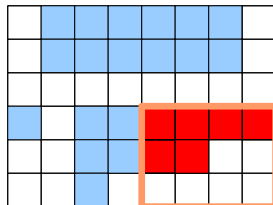
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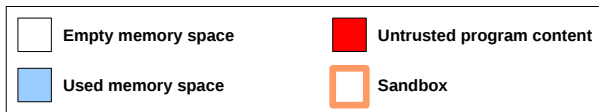
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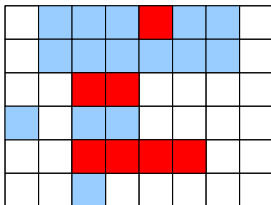
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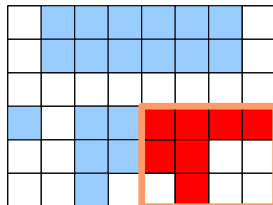
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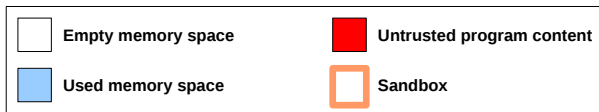
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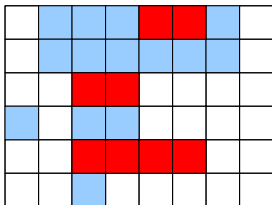
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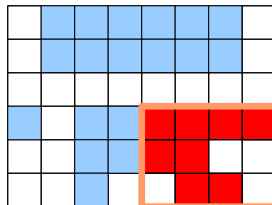
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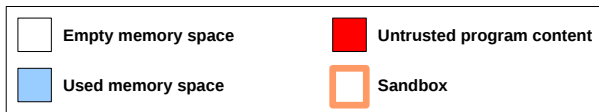
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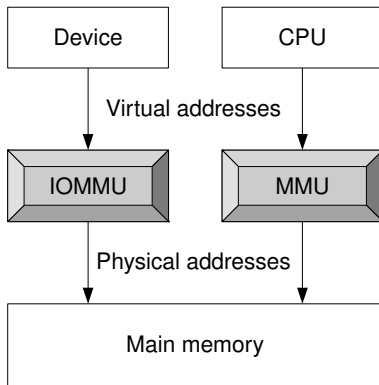
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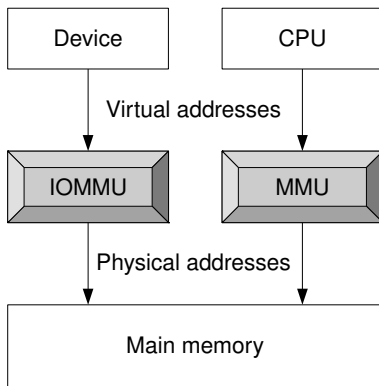
Memory (with sandbox)



Memory rights management



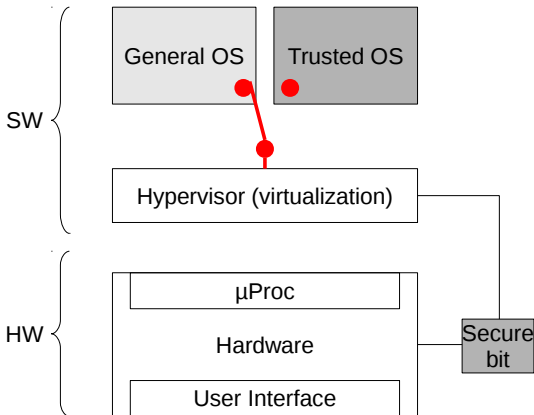
Memory rights management



→ **Vulnerabilities**

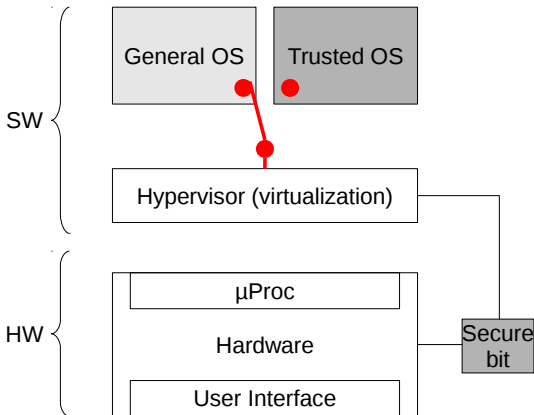
Virtual machines

example : TrustZone (ARM)



Virtual machines

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→ **Vulnerabilities**

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Conclusion and future works

- Complete protection : very difficult
 - Large attack surface : Bitstream → OS
 - Multidisciplinary skills : Avoid security holes
- RAM protection : high performance overhead
- OS : difficult to trust and certify

Conclusion and future works

Thank you for your attention !!!