Compact FPGA Implementations of Selected Round 3 SHA-3 Candidates

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CryptArchi 2011
Ruhr-Universität Bochum

Compact Implemtations

Already done:

- Skein, JH and Grøstl
- Evaluation currently for Virtex-5 FPGAs only

Near future:

- Implement BLAKE and Keccak
- Improve benchmarking
  - More platforms (Altera, Spartan-3, Spartan-6, Virtex-6, ...)
  - Usage of a modified XBX framework for automated benchmarking and power measurements
  - Report performance for short messages

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- Overall goal: Minimal area
- No usage of BlockRAMs, DSP units
- Include the padding function
- Identical hardware interface

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- Fast Simplex Link
- 32 bit wide unidirectional link with handshaking and an optional FIFO buffer

- 32 bit data signal
- *Master* FIFO full
- *Master* write
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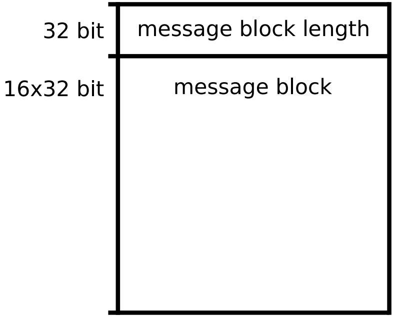
- Data format
- Message block length encoded in 32 bits
- Message block encoded with big endianess (512 bit=16x32 bit)



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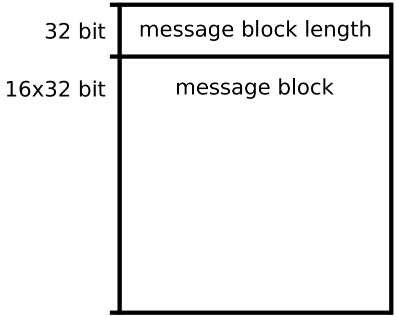

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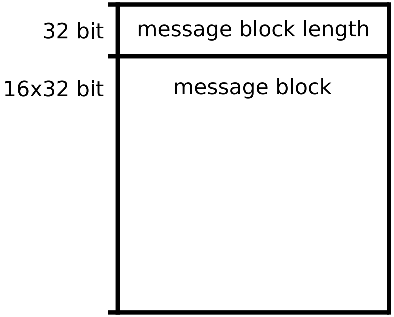
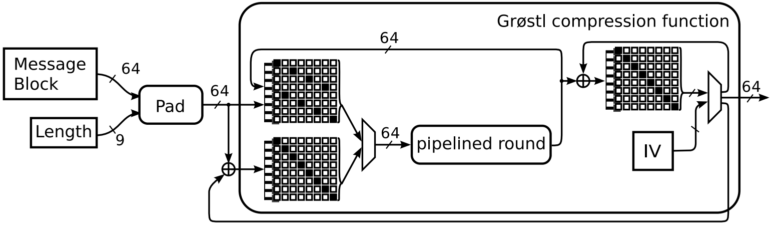


Grøstl - Design Overview



- Hardware for P and Q shared
- Distributed RAMs for P, Q and h

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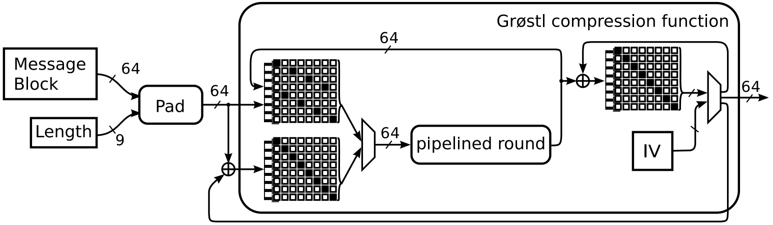

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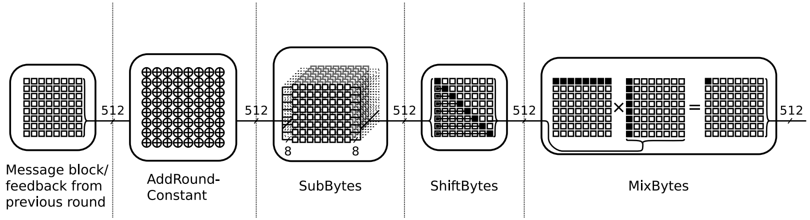

- 10 rounds
- Duplicated permutation (P and Q)

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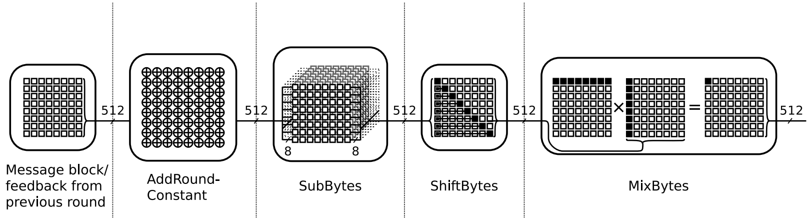

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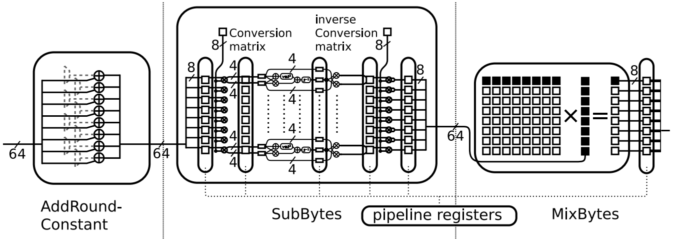

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- SubBytes implementation with composite field arithmetic

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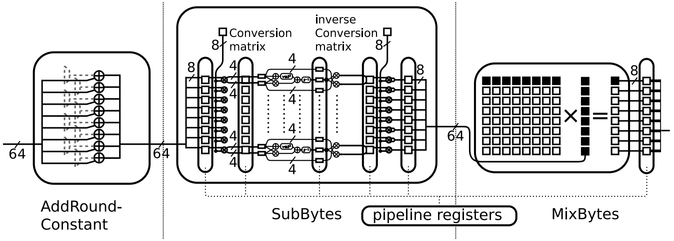

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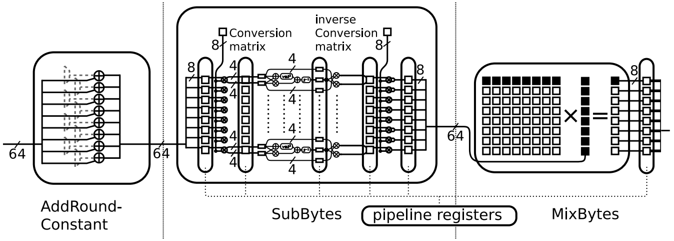

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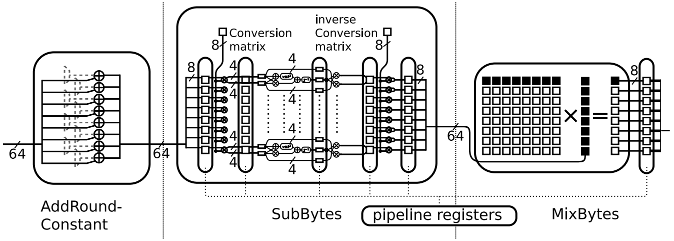

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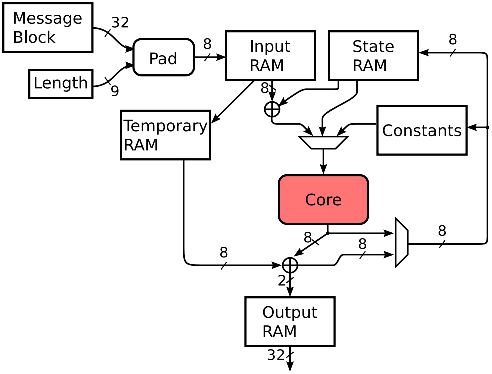

- Shared core for constants computation and round function

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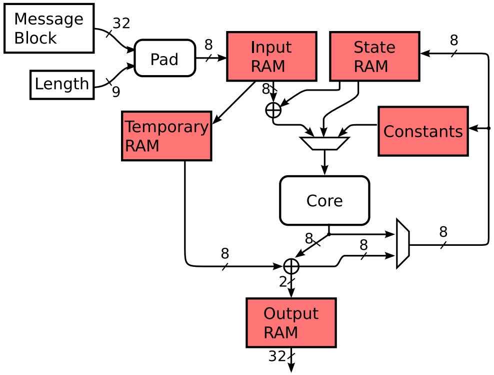

- RAMs for input, output, state, constants and a temp. buffer

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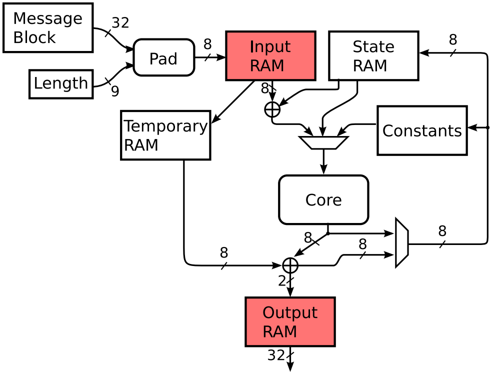

- Input and output RAMs do the grouping/de-grouping

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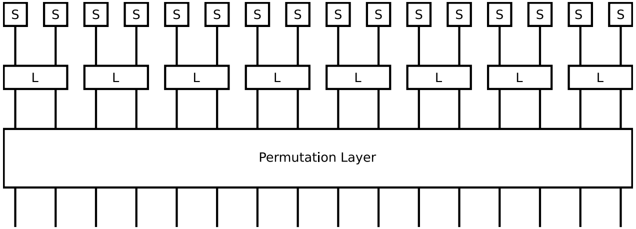

- S-Box, linear transformation and permutation
- Simpler transformations than Grøstl and thus faster per round
- But ... 42 rounds

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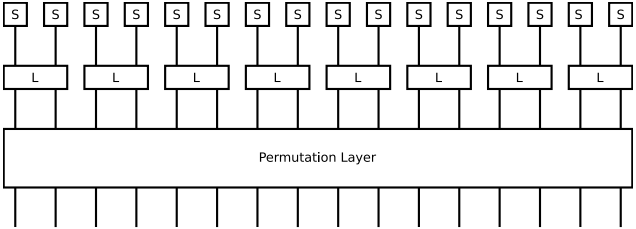

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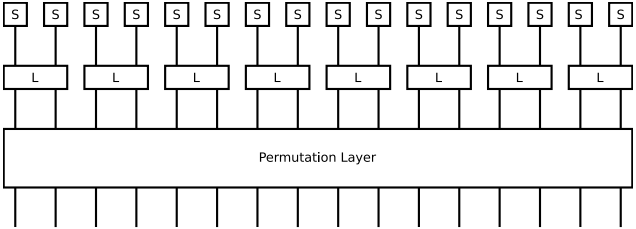

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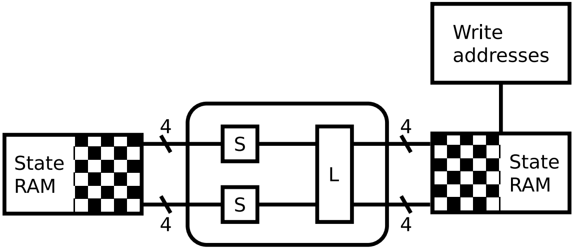

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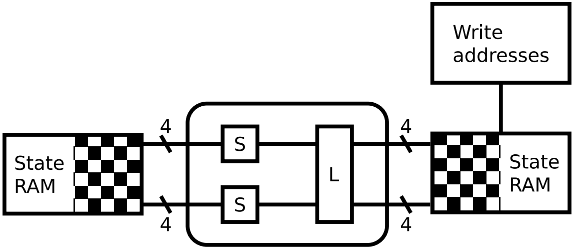

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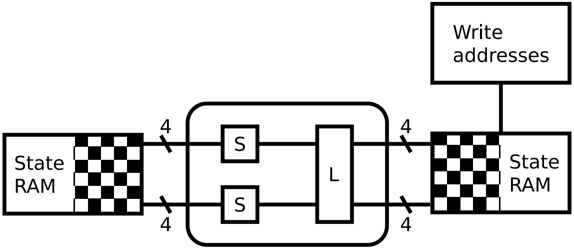

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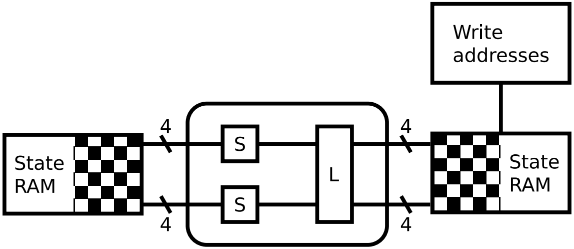

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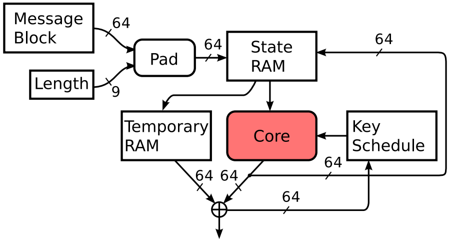

- Minimized, pipelined core (partial round function)

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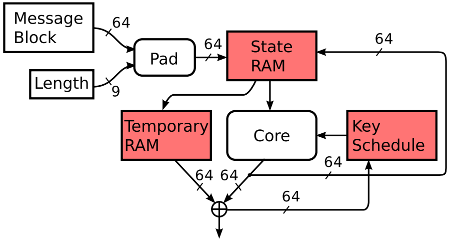
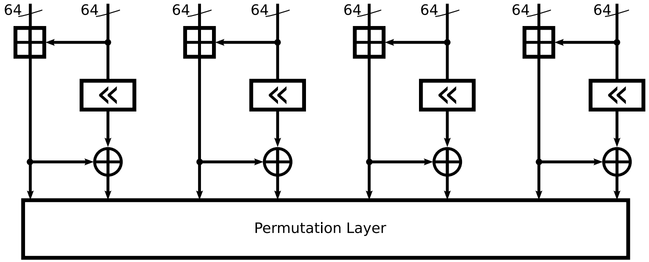


- RAMs for hash state, key schedule and a temporary buffer.

Skein - Round Function



- 72 rounds
- Key injection (addition in 64 bit blocks) every 4th round

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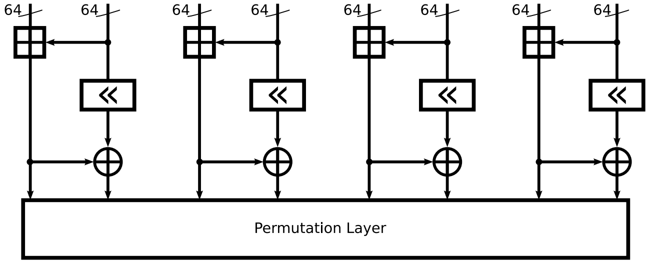

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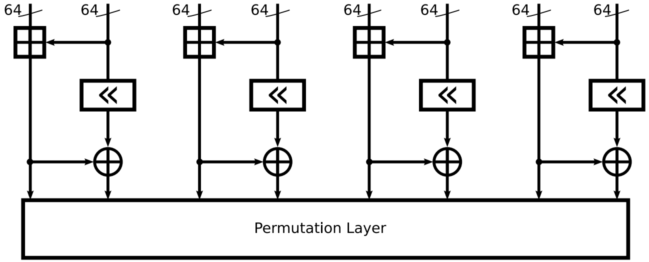

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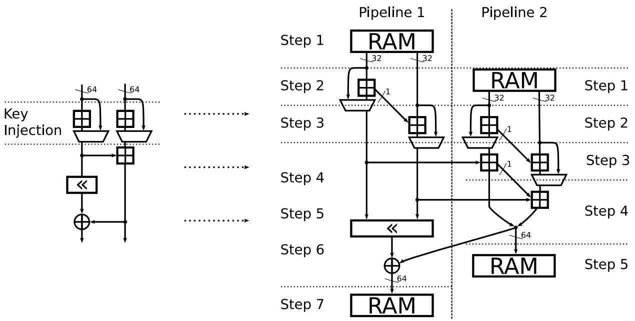

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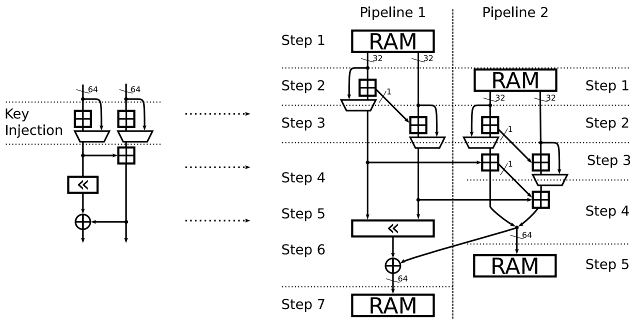

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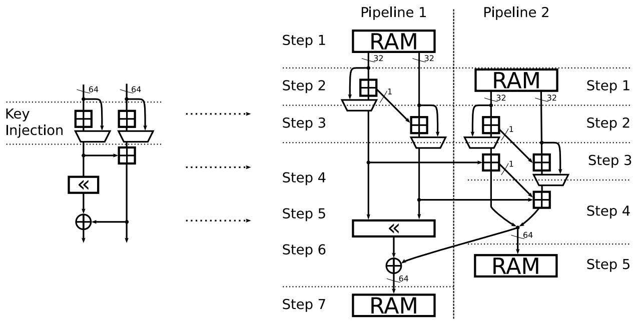

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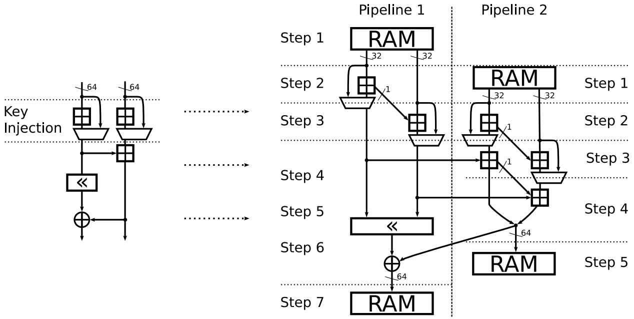

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Grøstl	470	354	**1132**	**2.40**
JH	**205**	341	27	0.13
Skein	555	271	237	0.42

Table: Results for Virtex-5 FPGAs

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- Xilinx ISE 12.3
- Optimized parameters for timing performance and area (xst, map, par)

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- JH is flexible, too, but:
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