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High Throughput TRNGs on FPGAs

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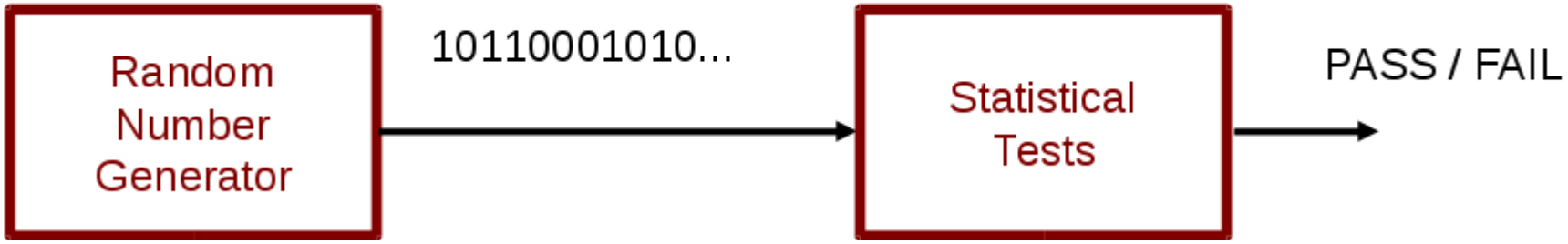
ESAT-COSIC and iMinds, KU Leuven

Outline

- Design and Evaluation Requirements
- Entropy Extraction
- General Architecture
- Stochastic Model
- Platform Parameters
- Design Decisions
- Results
- Conclusions and Future Work

Security Evaluation

THE OLD METHOD:



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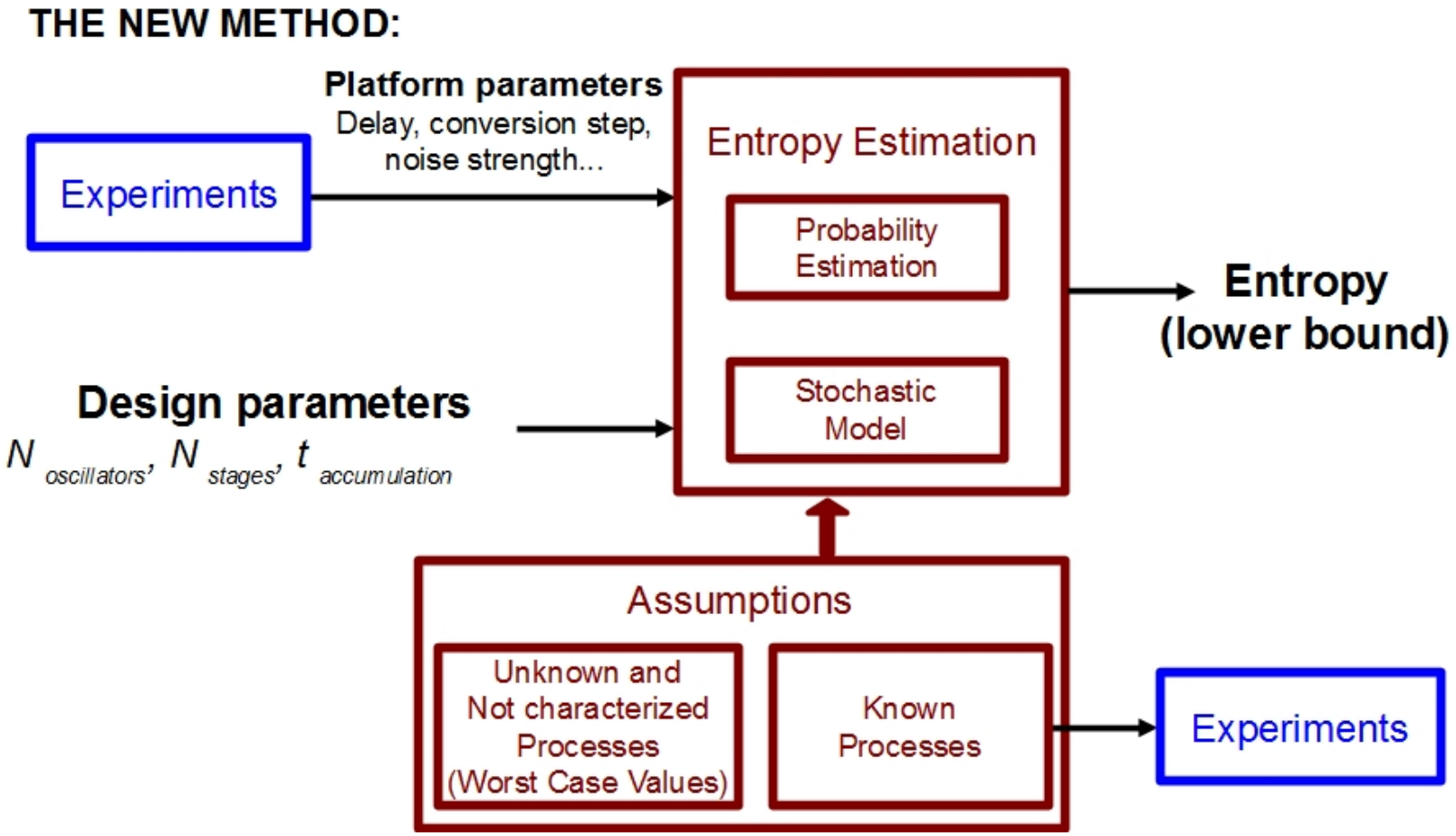
Security Evaluation



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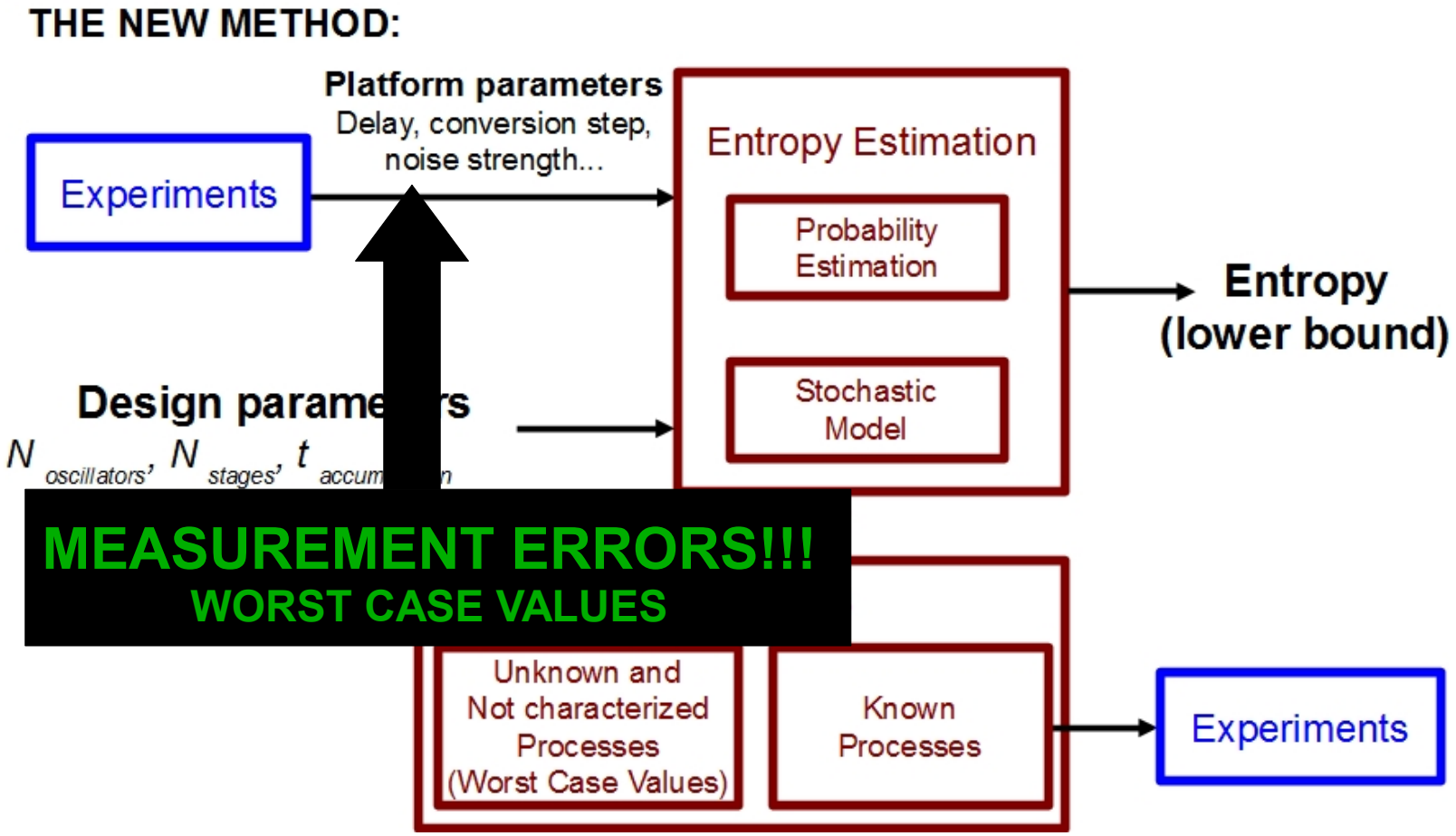
Security Evaluation



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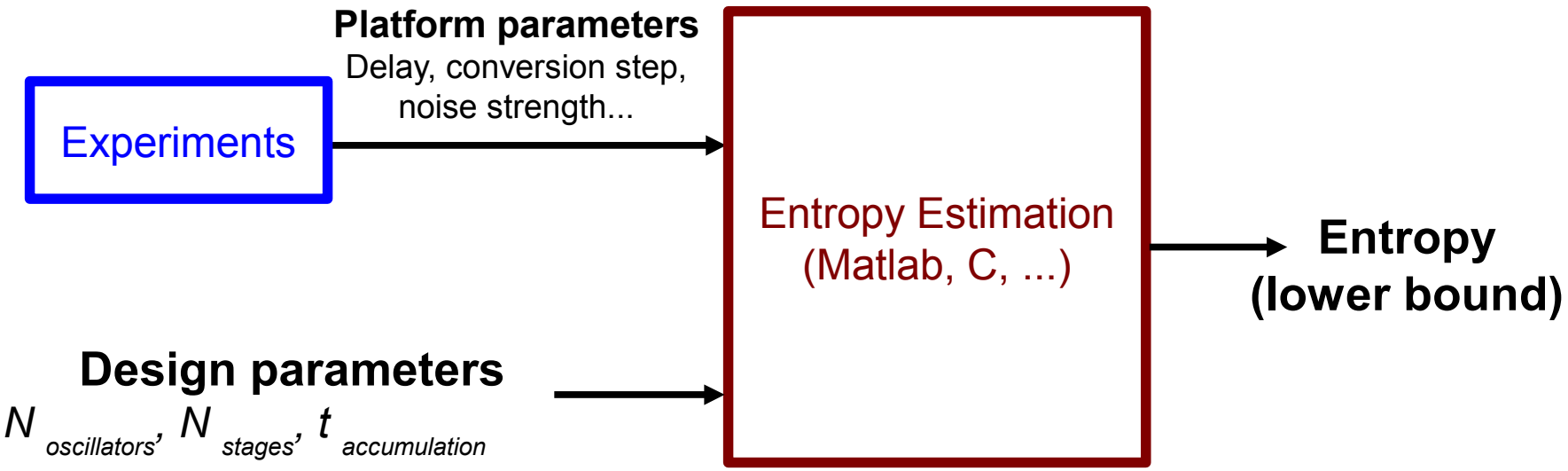
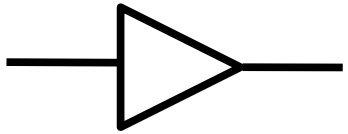
Design Procedure



- STEP1: Build the mathematical model for estimating entropy
- STEP2: Measure the relevant platform parameters
- STEP3: Tune design parameters to make trade-offs

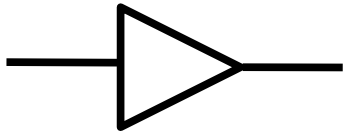
Timing Jitter

Delay=d0+Δd



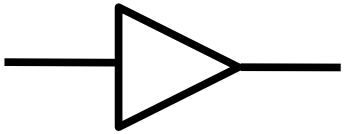
Timing Jitter

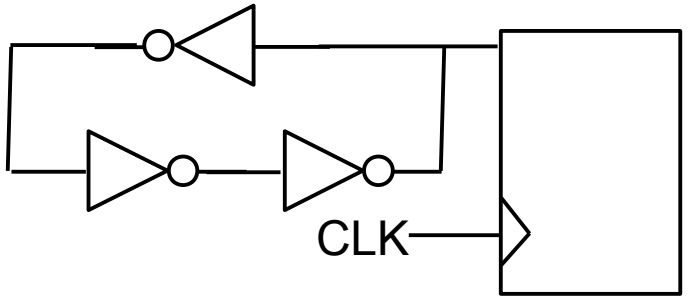
Delay=d0+Δd RANDOM

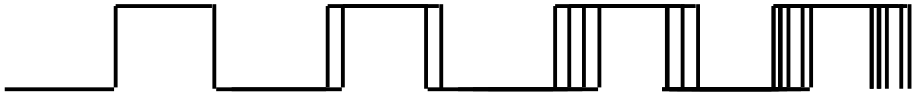


Timing Jitter

Delay=d0+Δd RANDOM







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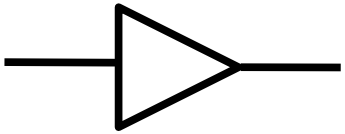
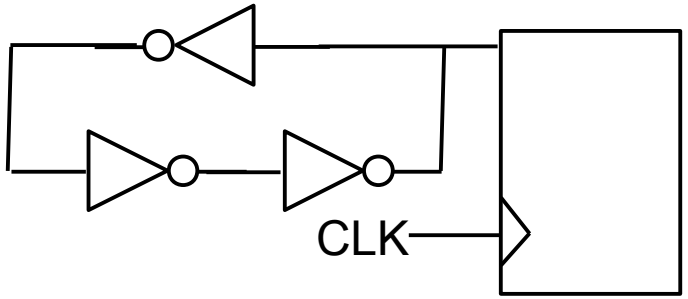
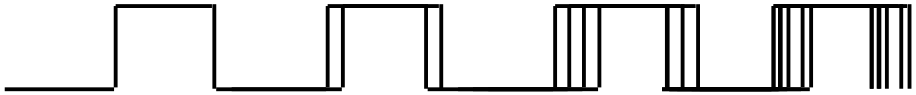
Timing Jitter

Delay=d0+Δd RANDOM



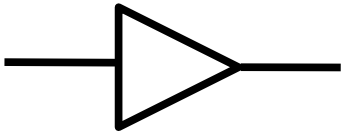


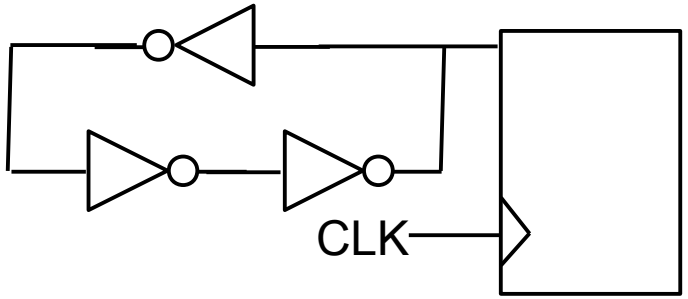


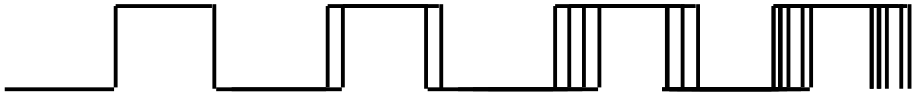
More
Oscillators

Timing Jitter

Delay=d0+Δd RANDOM





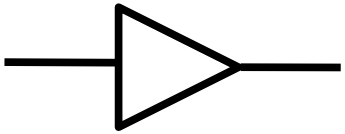


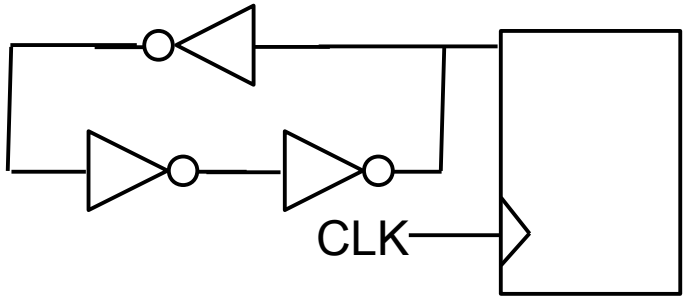
More Oscillators

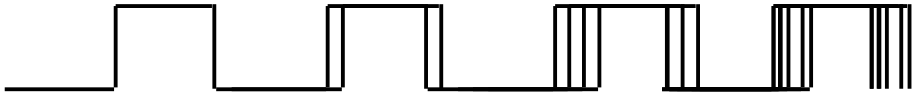
More Transitions

Timing Jitter

Delay=d0+Δd RANDOM







More Oscillators

More Transitions

Efficient Entropy Extraction

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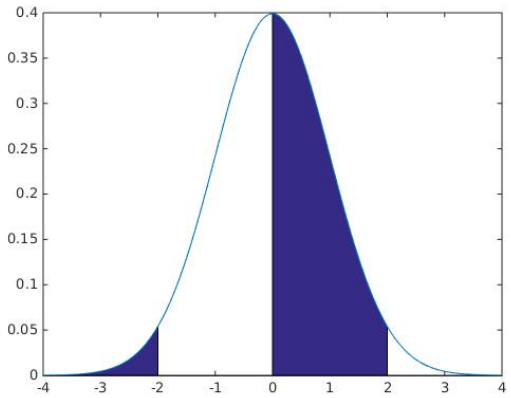
Entropy Extraction



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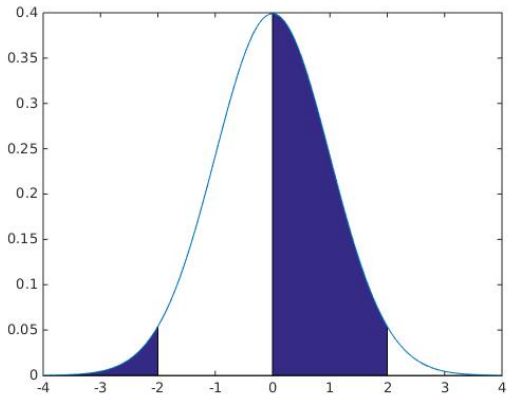
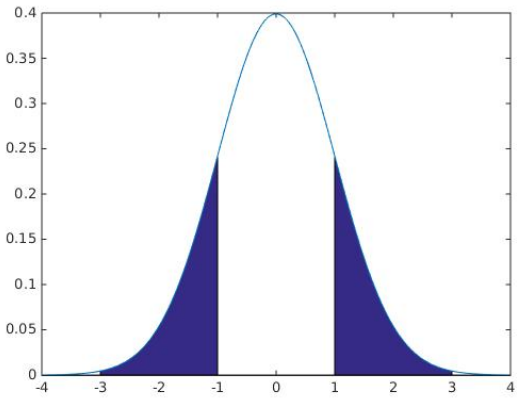
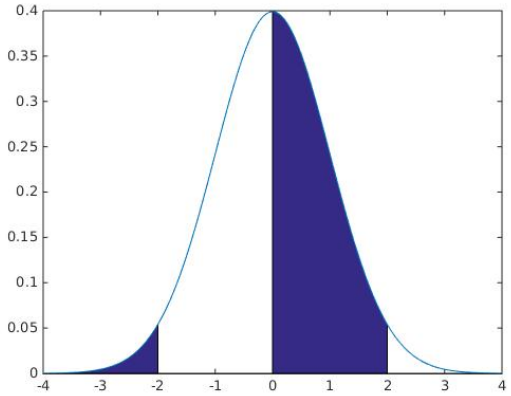
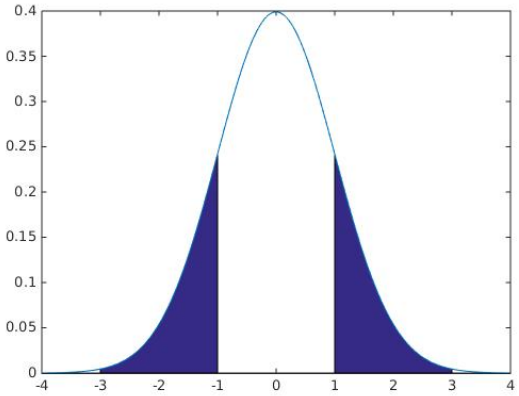
Entropy Extraction

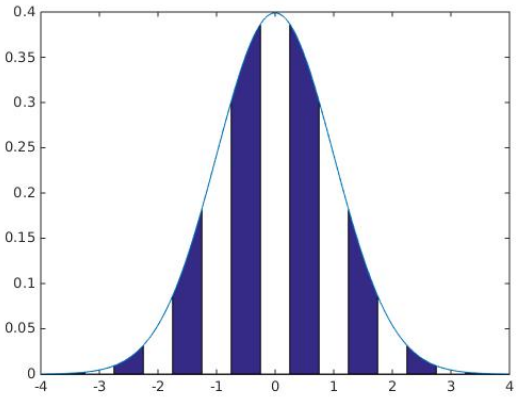




Entropy Extraction







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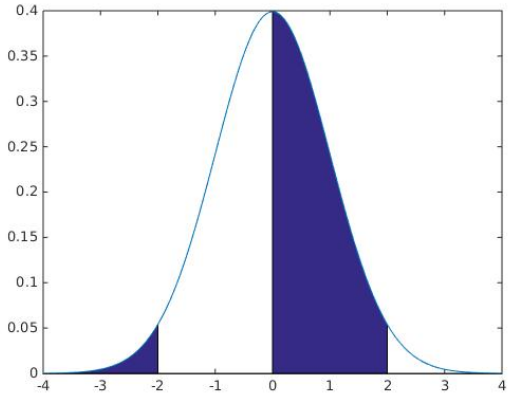
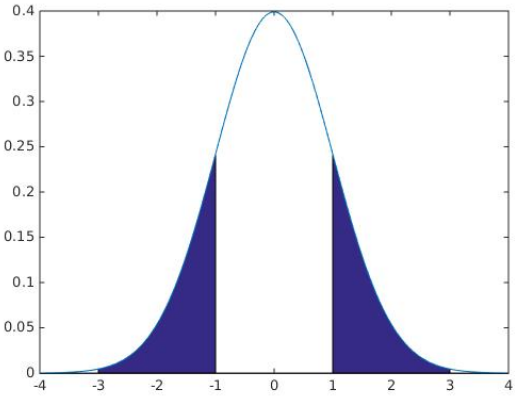
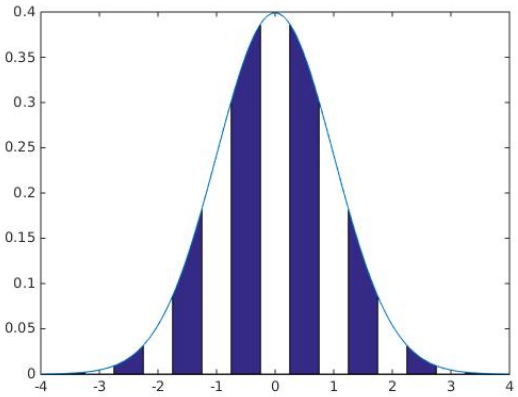
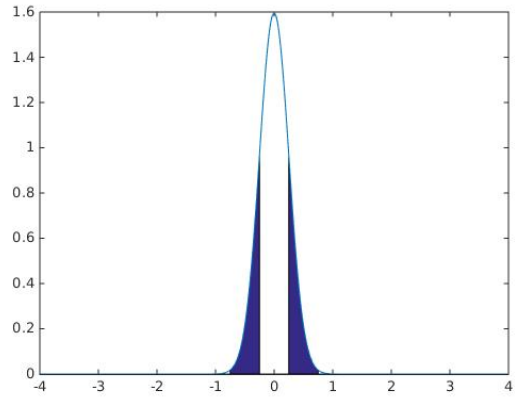
Entropy Extraction









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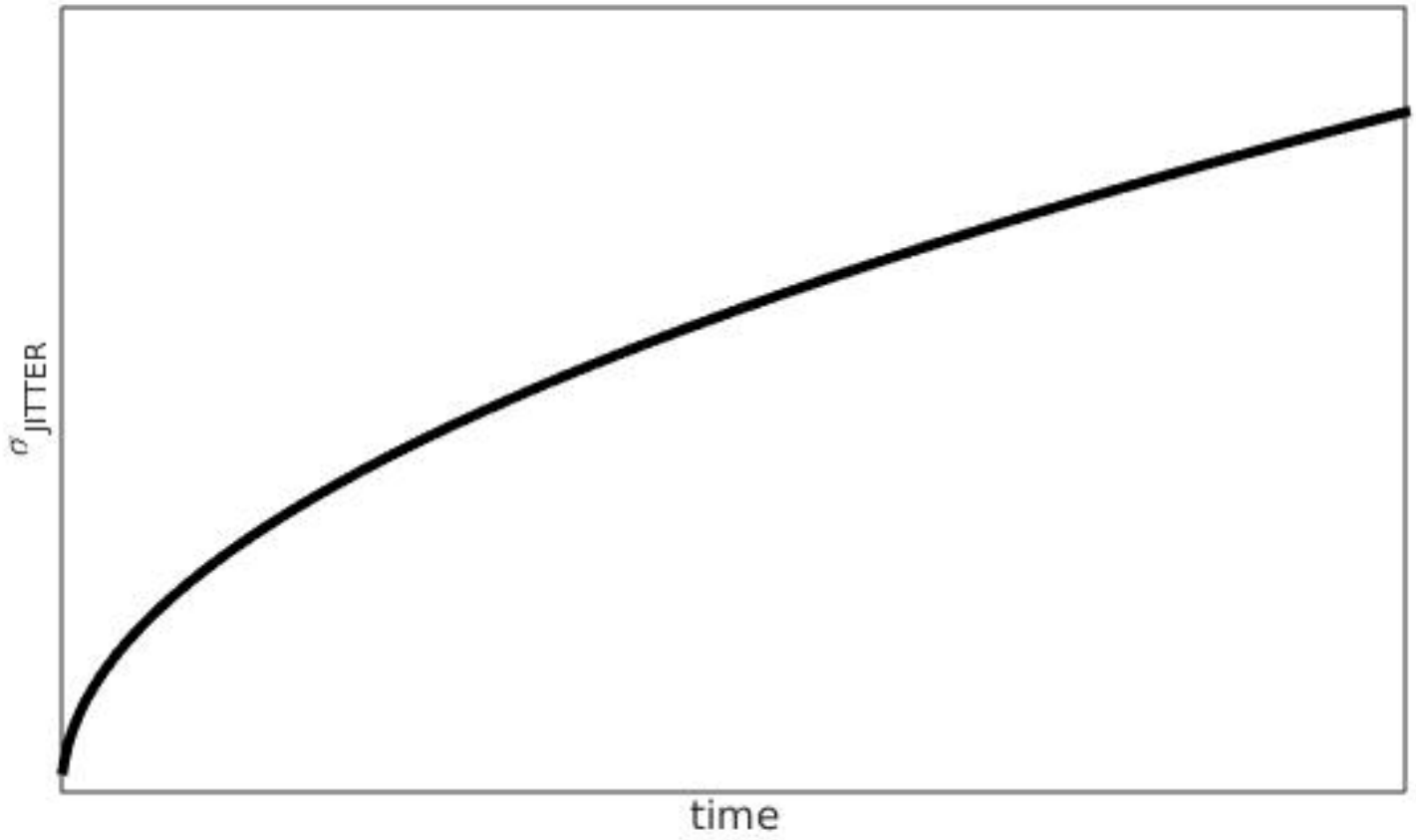
Jitter Accumulation



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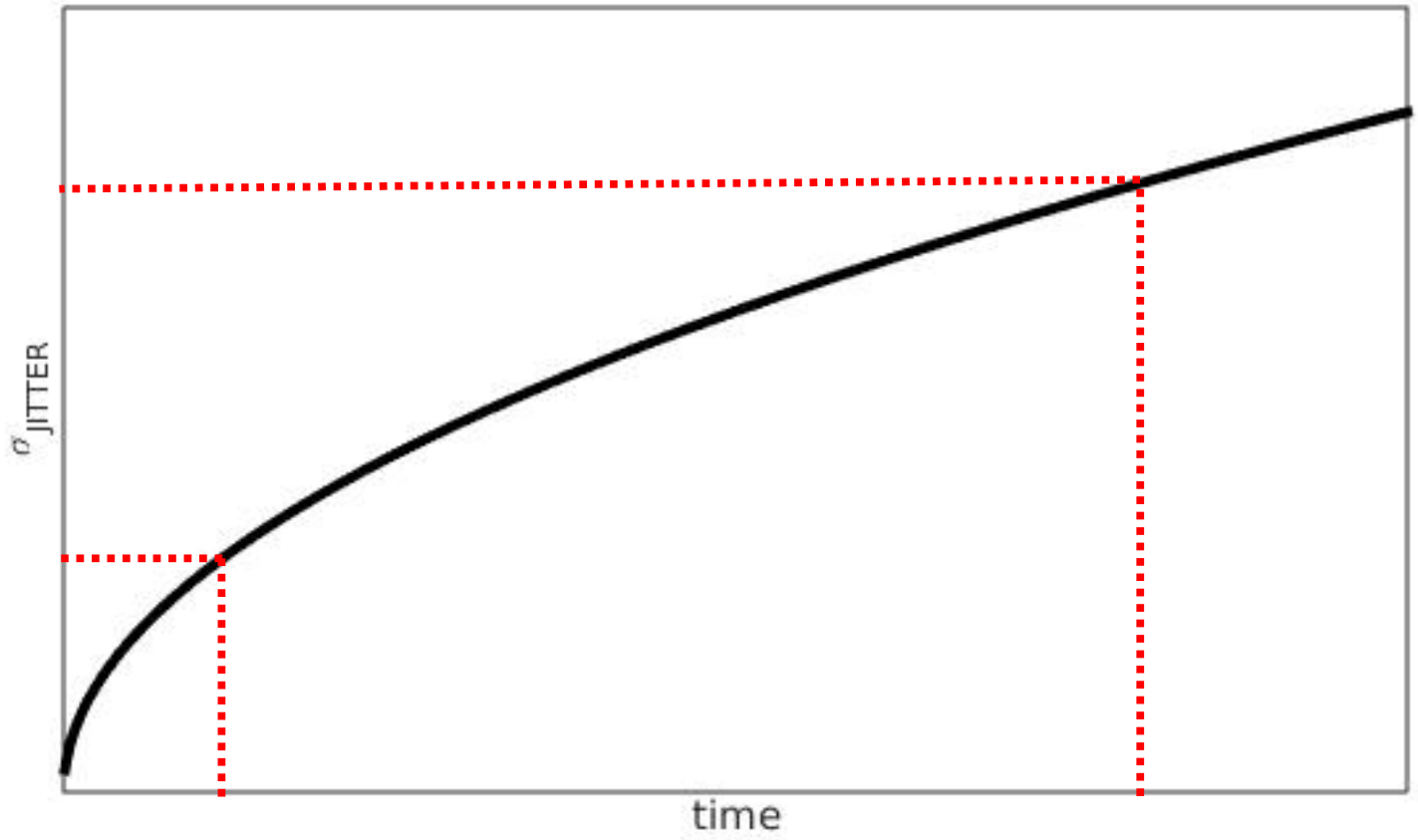
Jitter Accumulation



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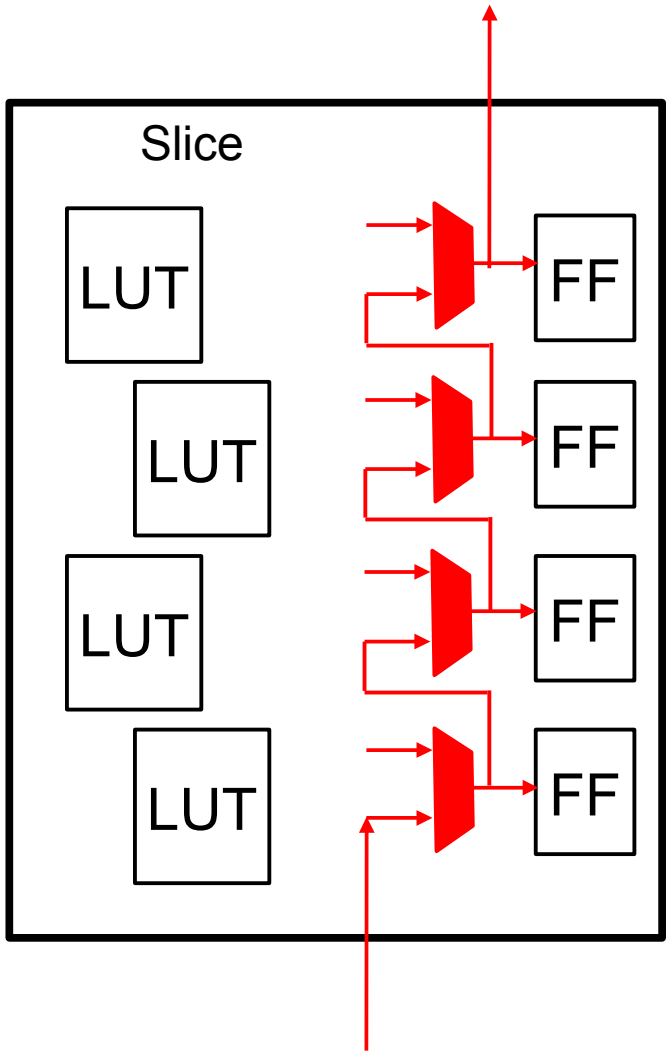
Entropy Extraction on FPGA



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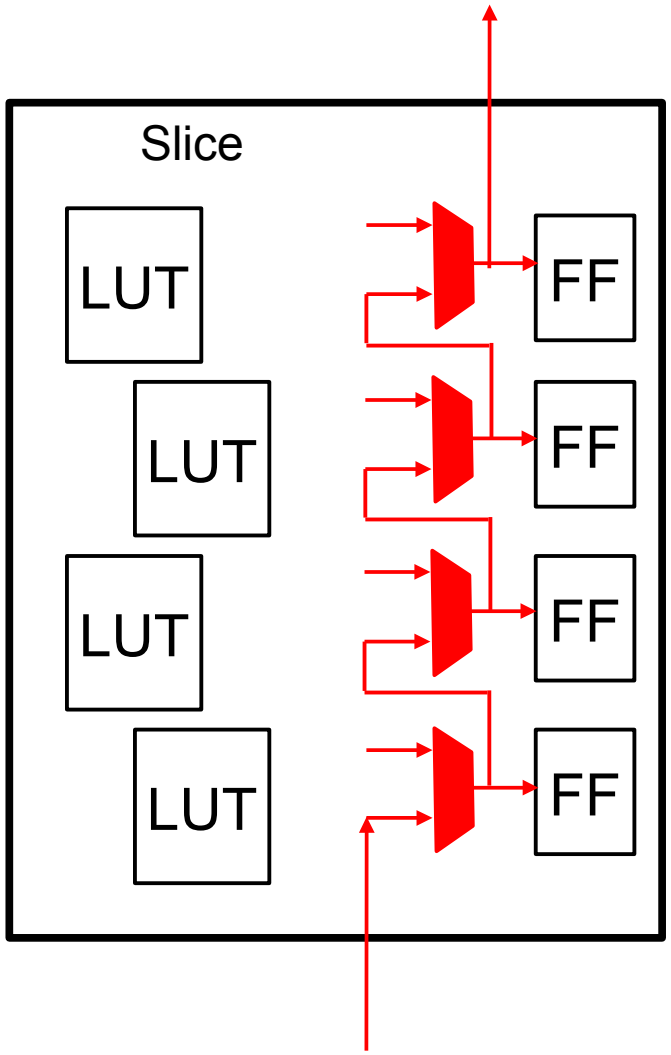
Entropy Extraction on FPGA



d_{step}=16ps to 17ps

d_{LUT}=480ps

$(d_{LUT}/d_{step})^2$=797.2

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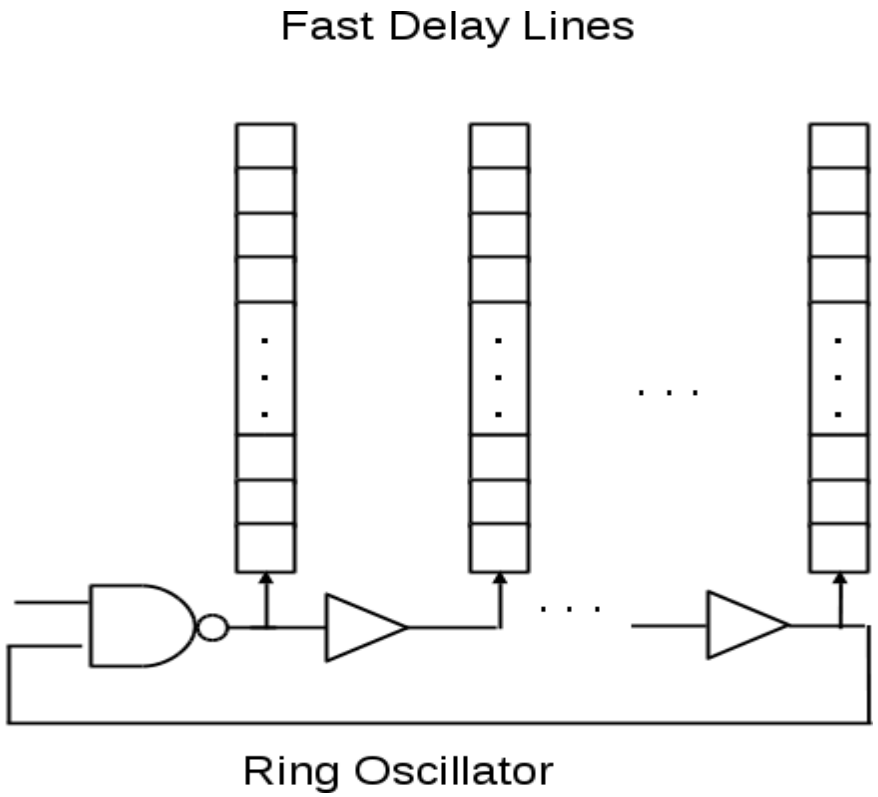
Entropy Source

V. Rozic, B. Yang, W. Dehaene and I. Verbauwhede, “Highly-Efficient Entropy Extraction for True Random Number Generators on FPGAs”, DAC 2015.



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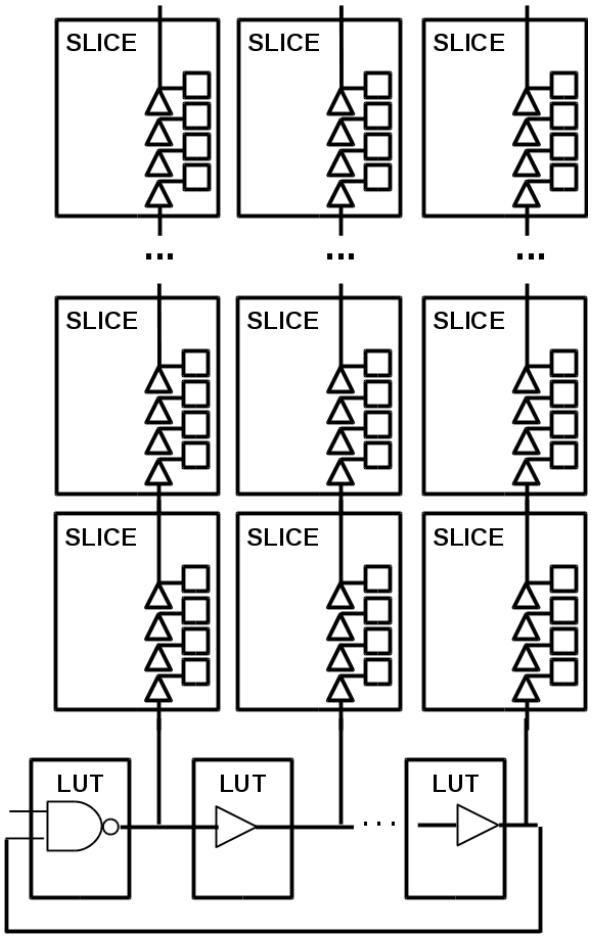
Entropy Source - Implementation



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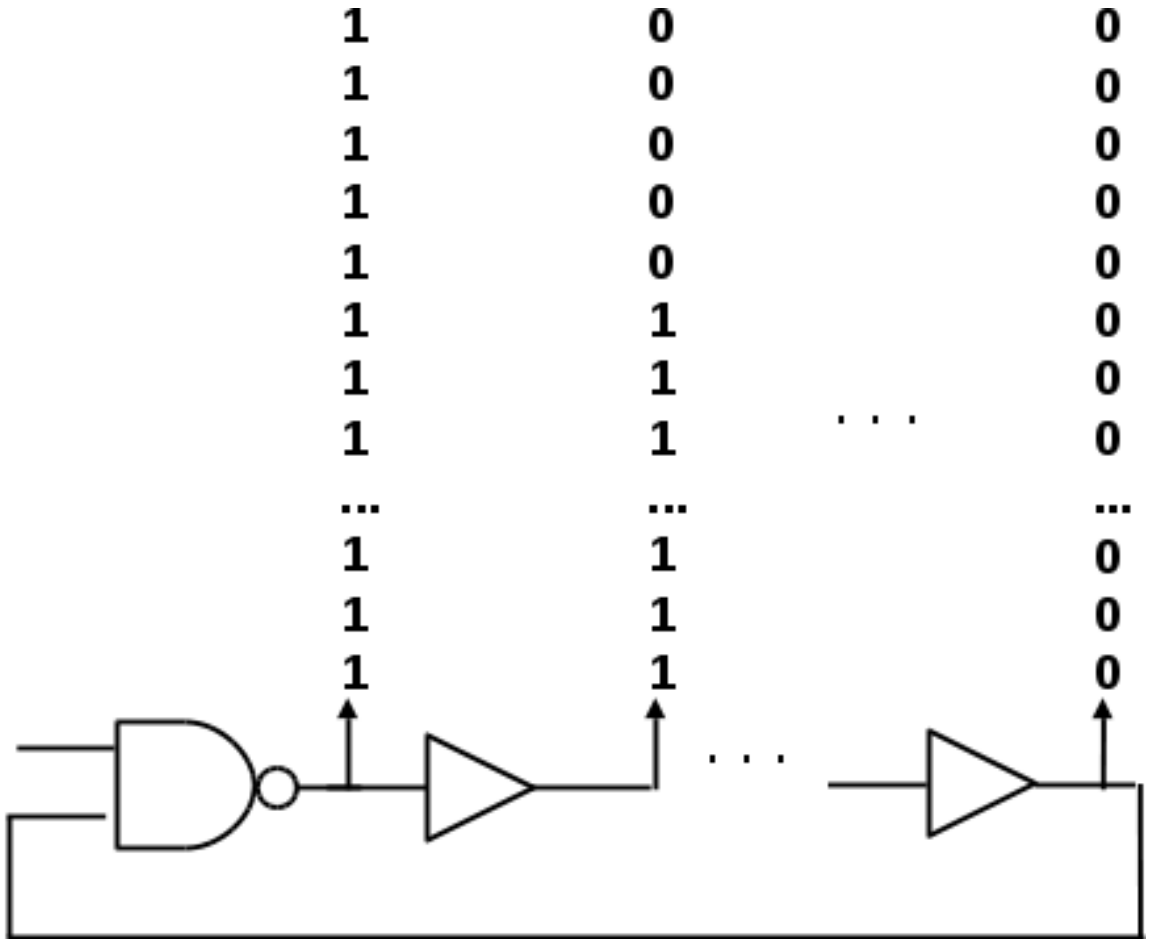
Jitter Snapshot



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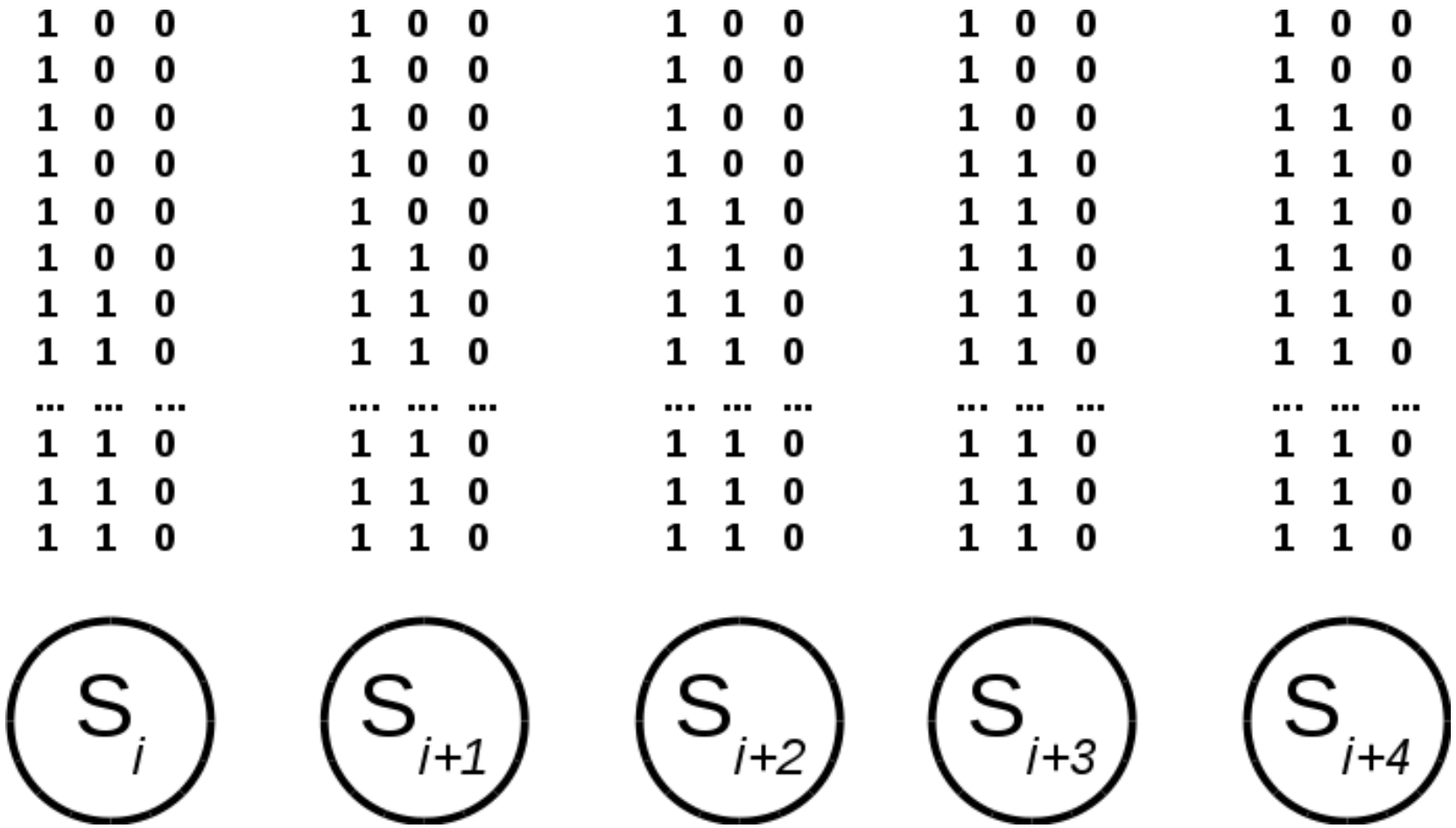
Stochastic Model - FSM



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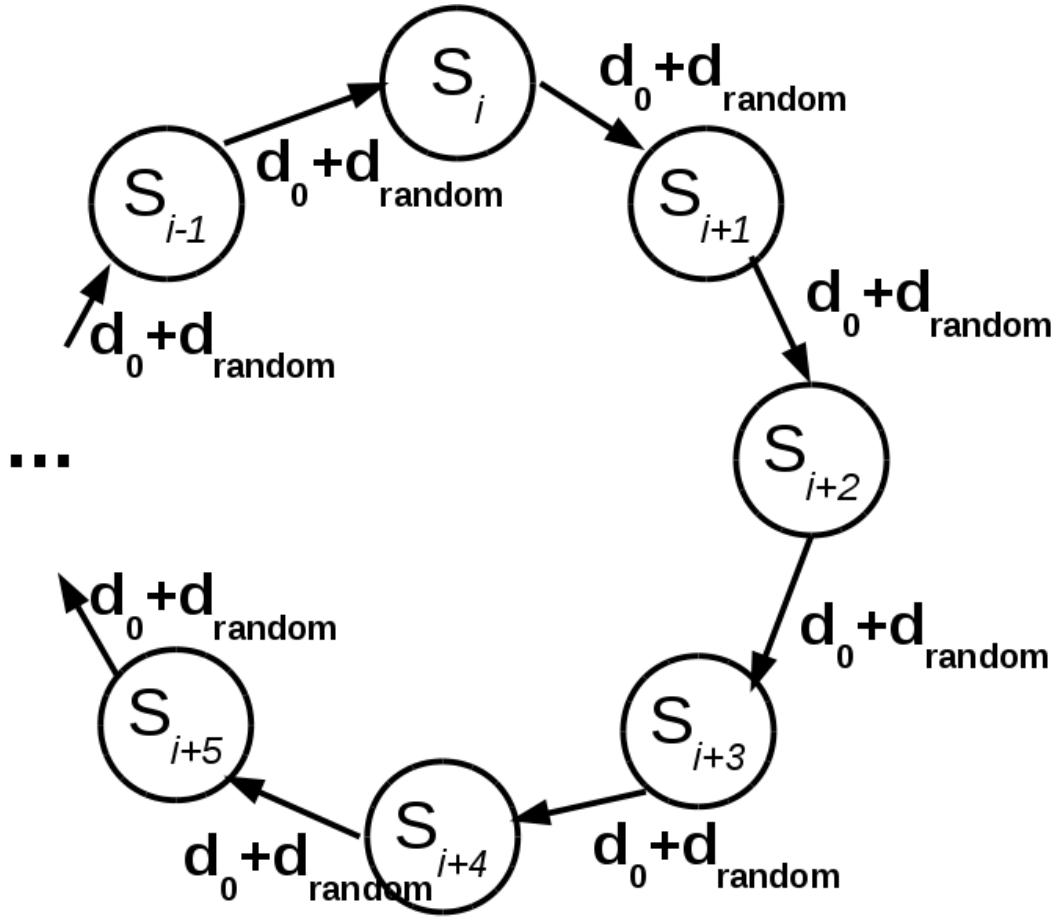
Stochastic Model - FSM



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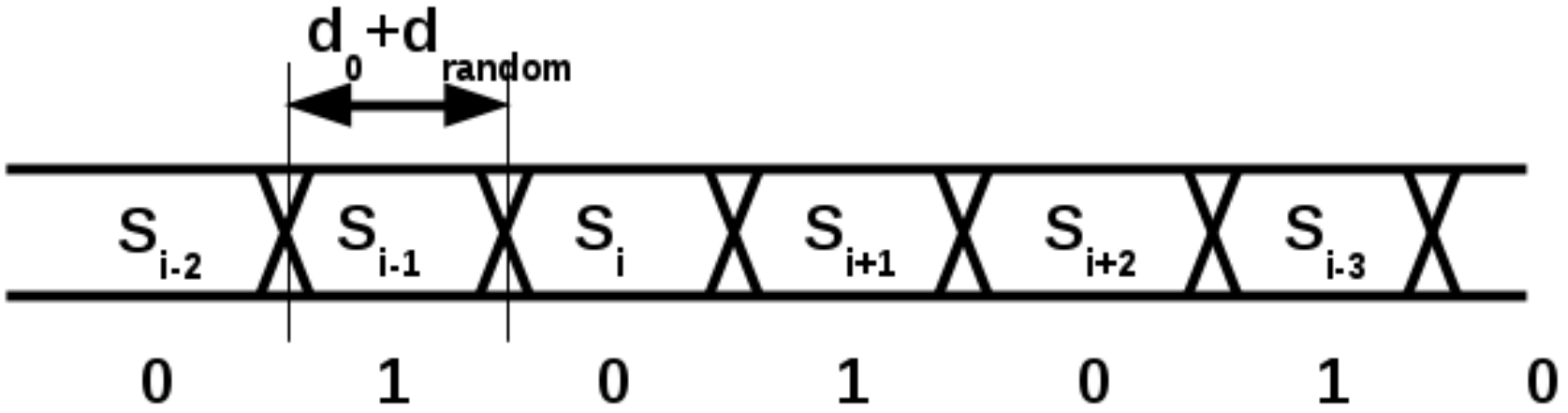
Stochastic Model - FSM



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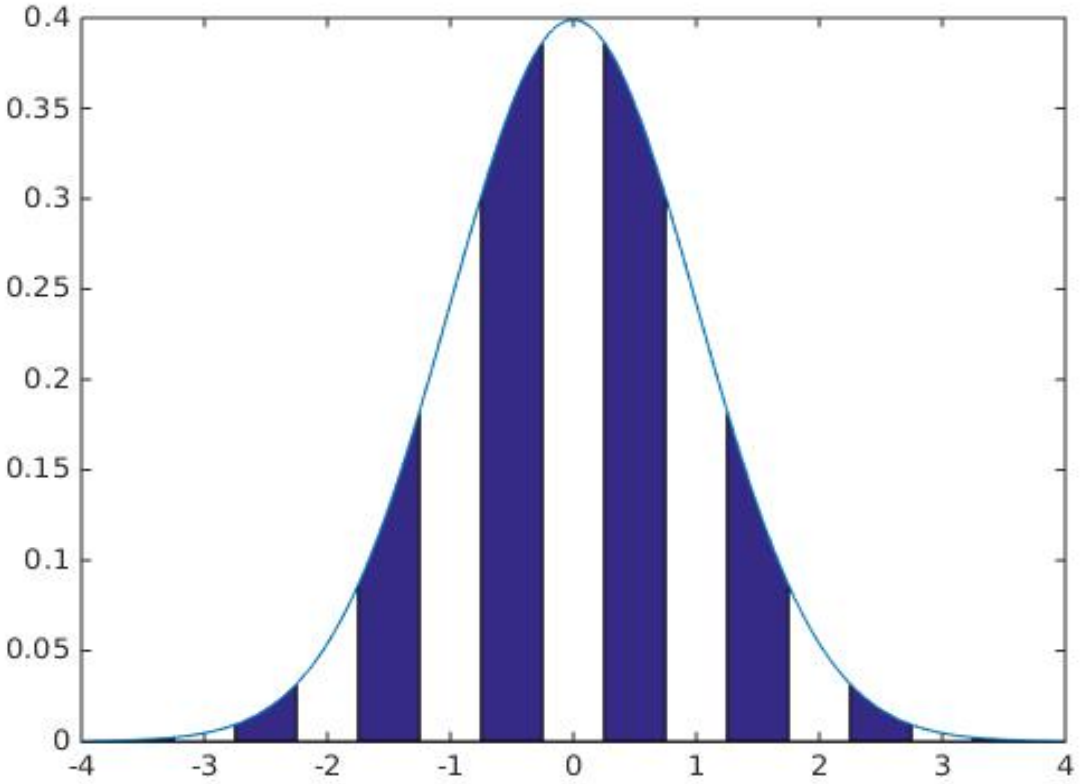
Binary Probability



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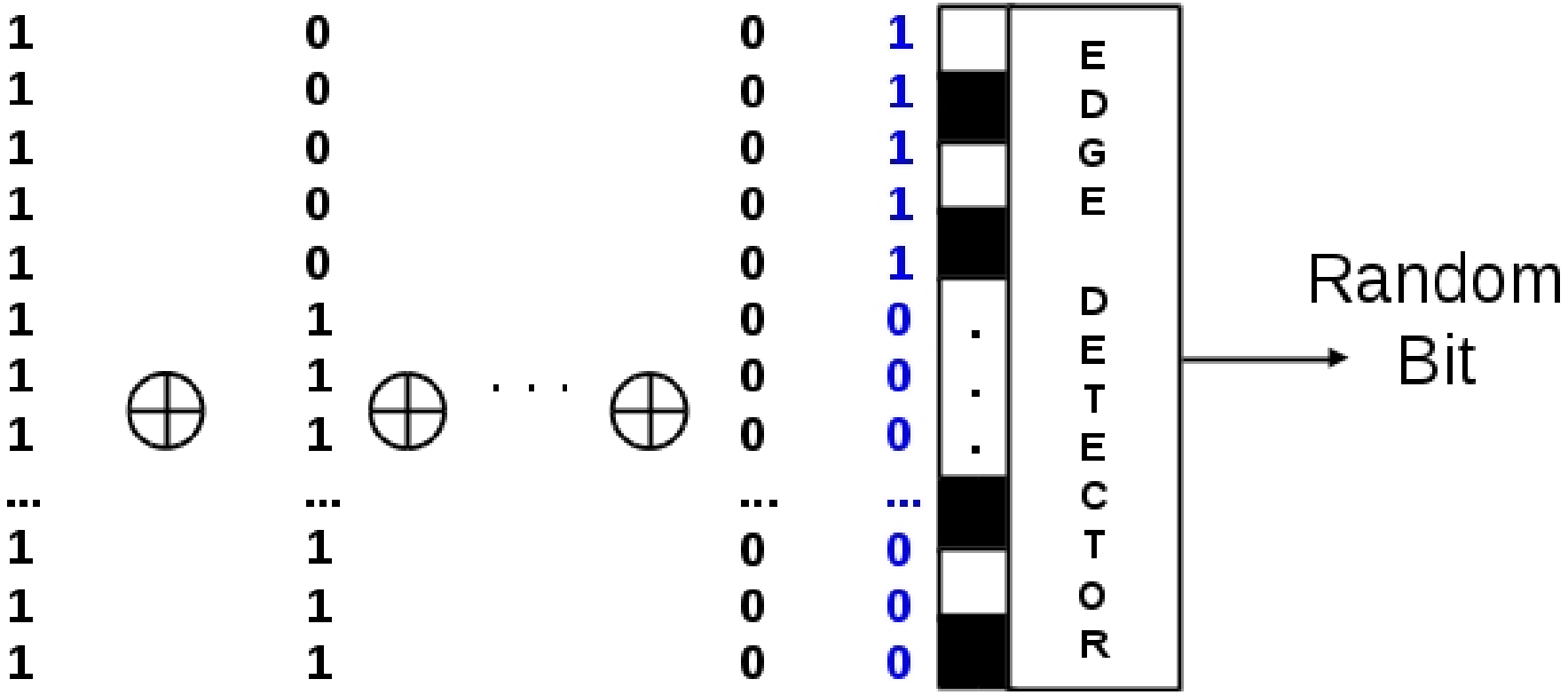
Entropy Extraction - Edge Position Decoding



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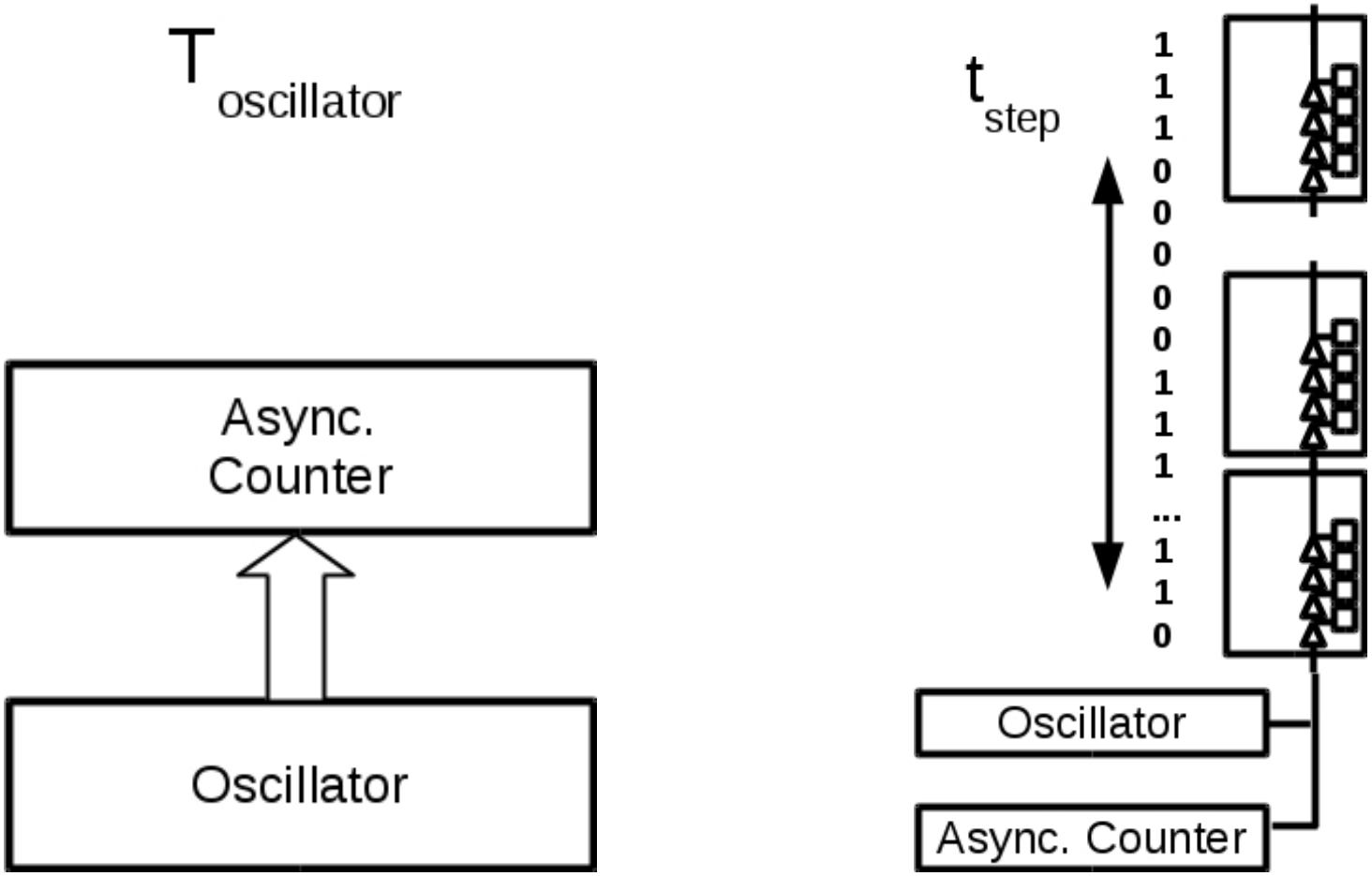
Platform Parameters



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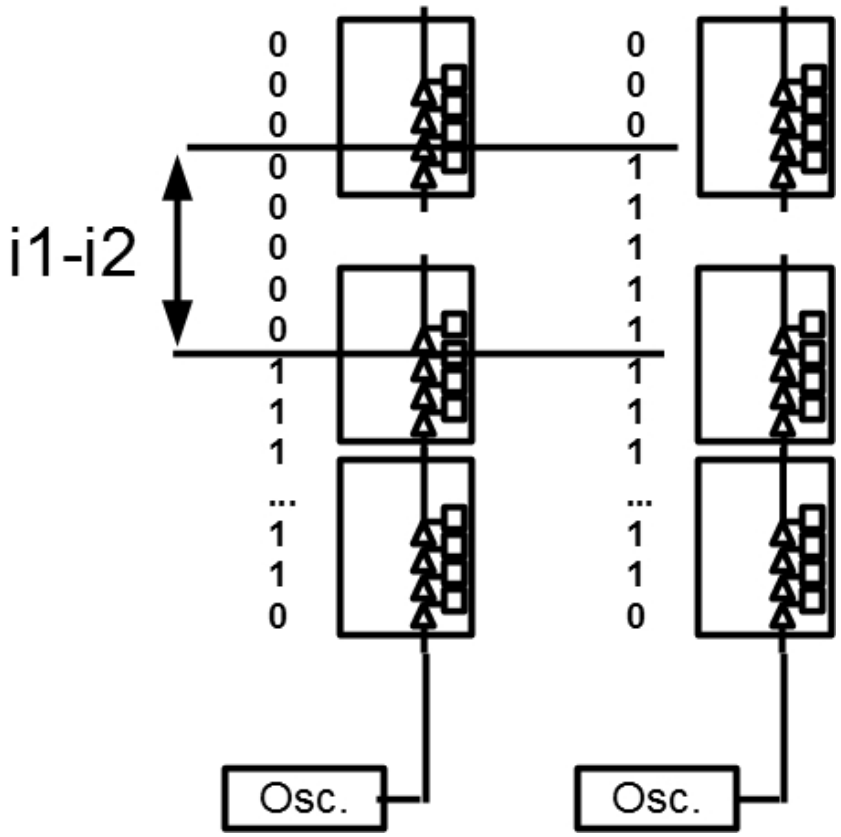
Platform Parameters-Jitter



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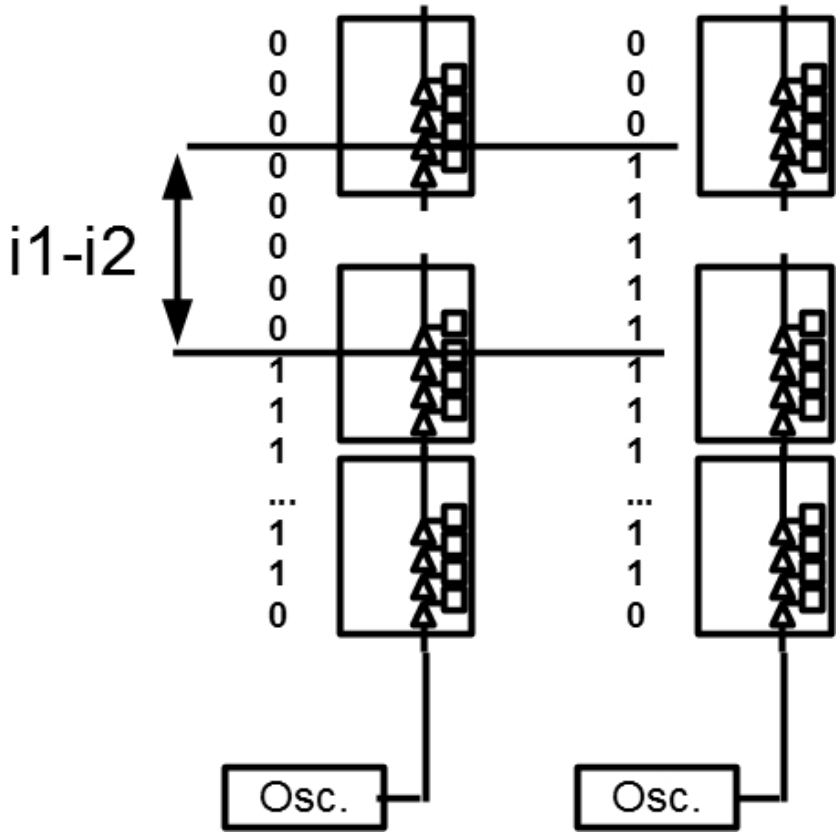
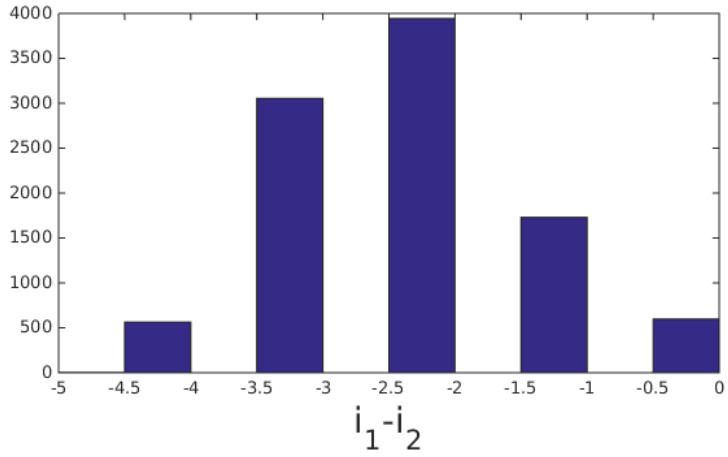
Platform Parameters-Jitter





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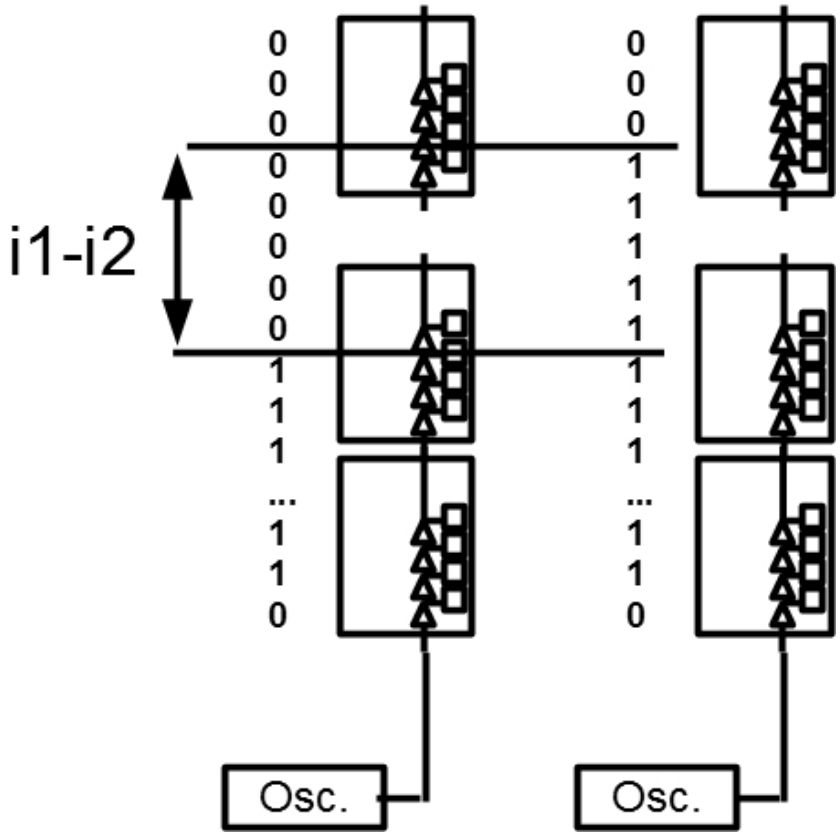
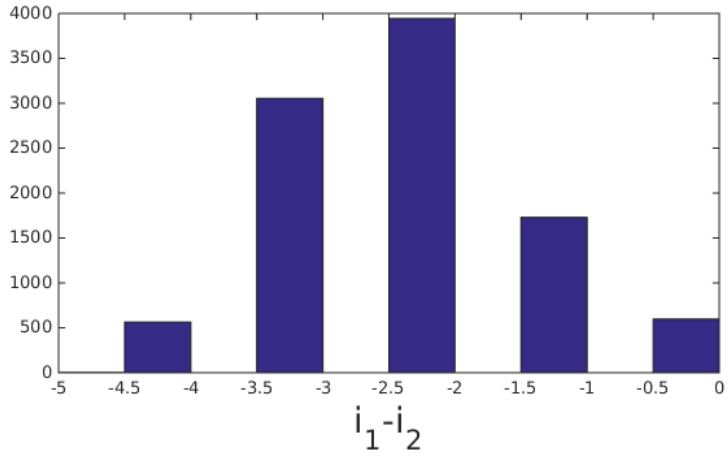
Platform Parameters-Jitter





t=20ns

σ_{jitter}=0.97 * 16ps = 15.5 ps

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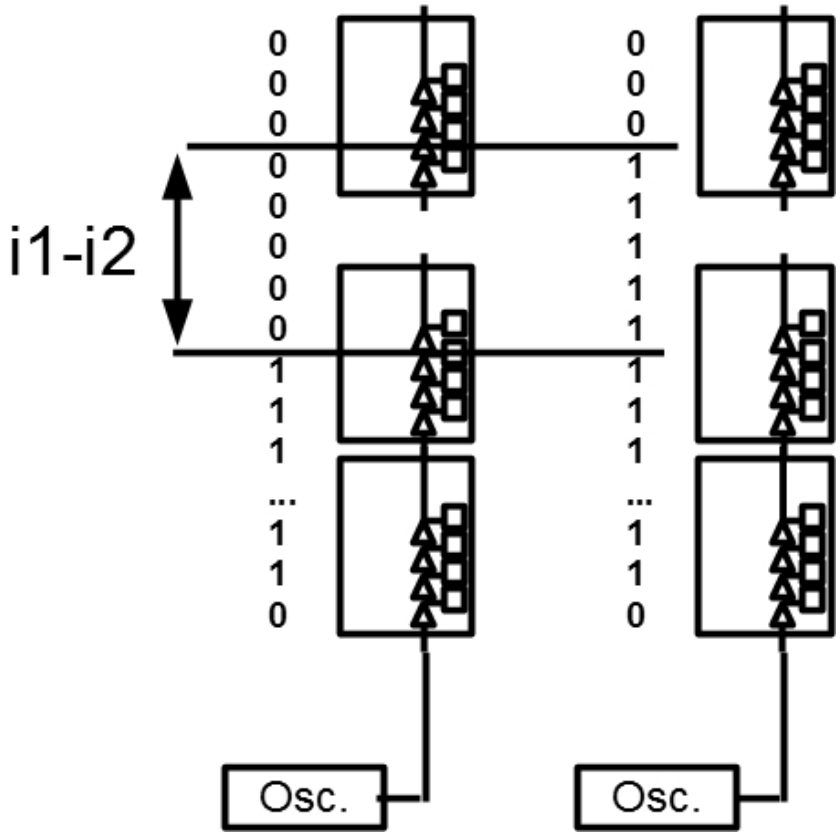
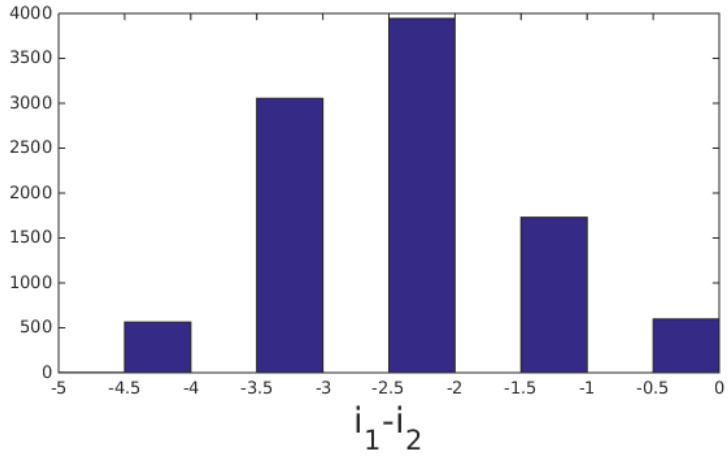
Platform Parameters-Jitter





t=20ns

σ_{jitter}=0.97 * 16ps = 15.5 ps

-20%

12.5 ps

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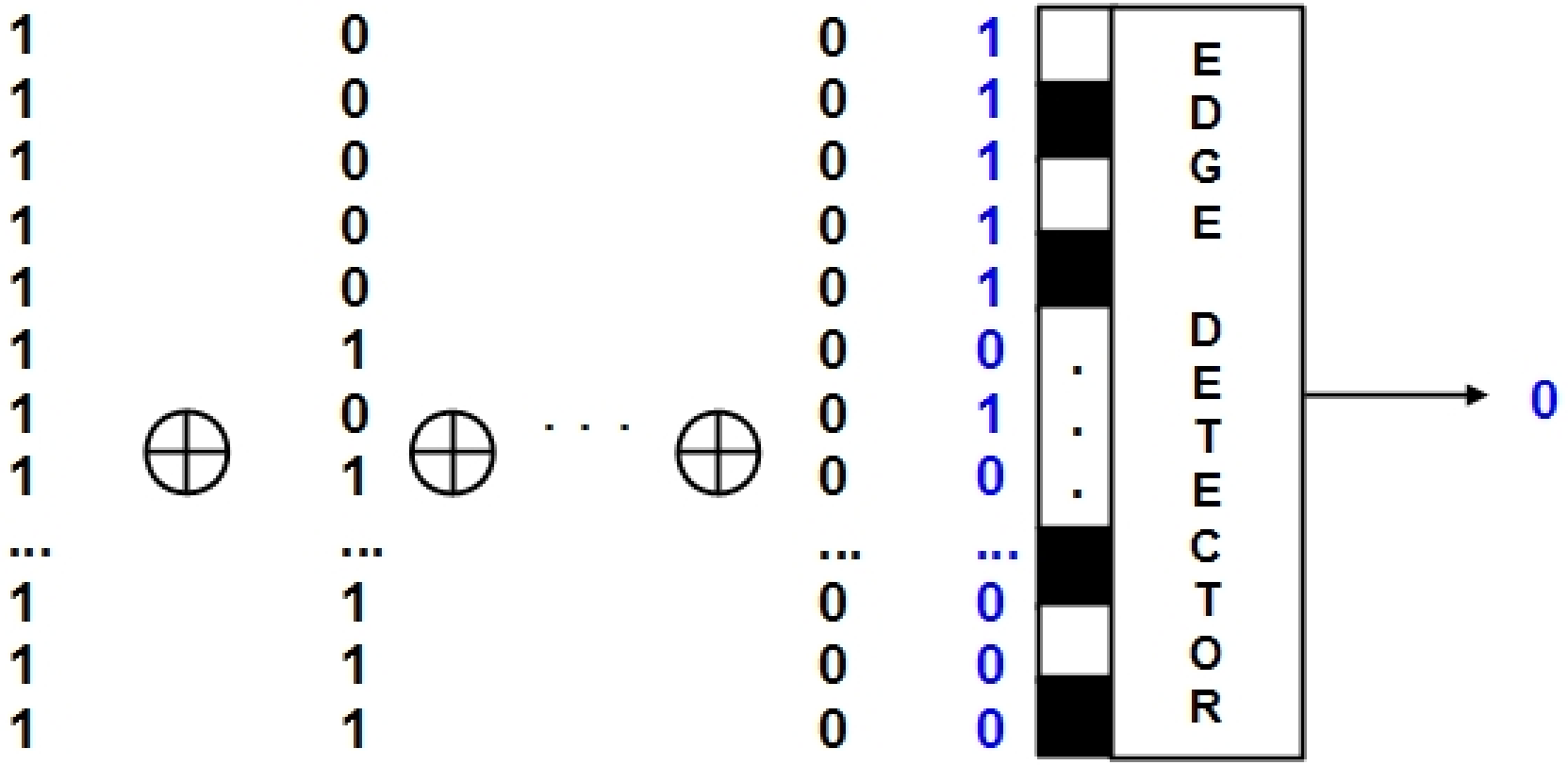
Entropy Extraction - Bubbles in the Code



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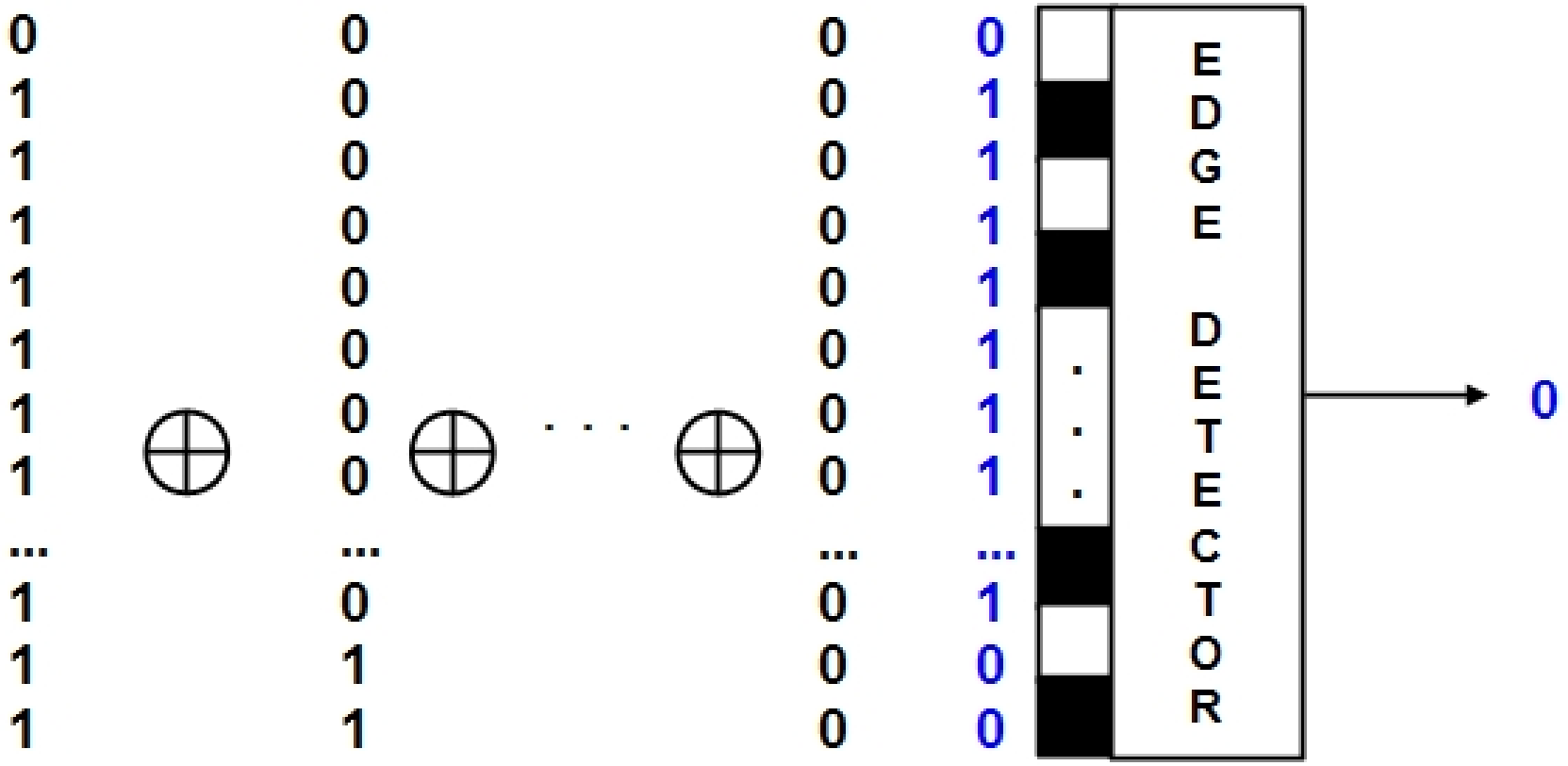
Entropy Extraction – Double Edges



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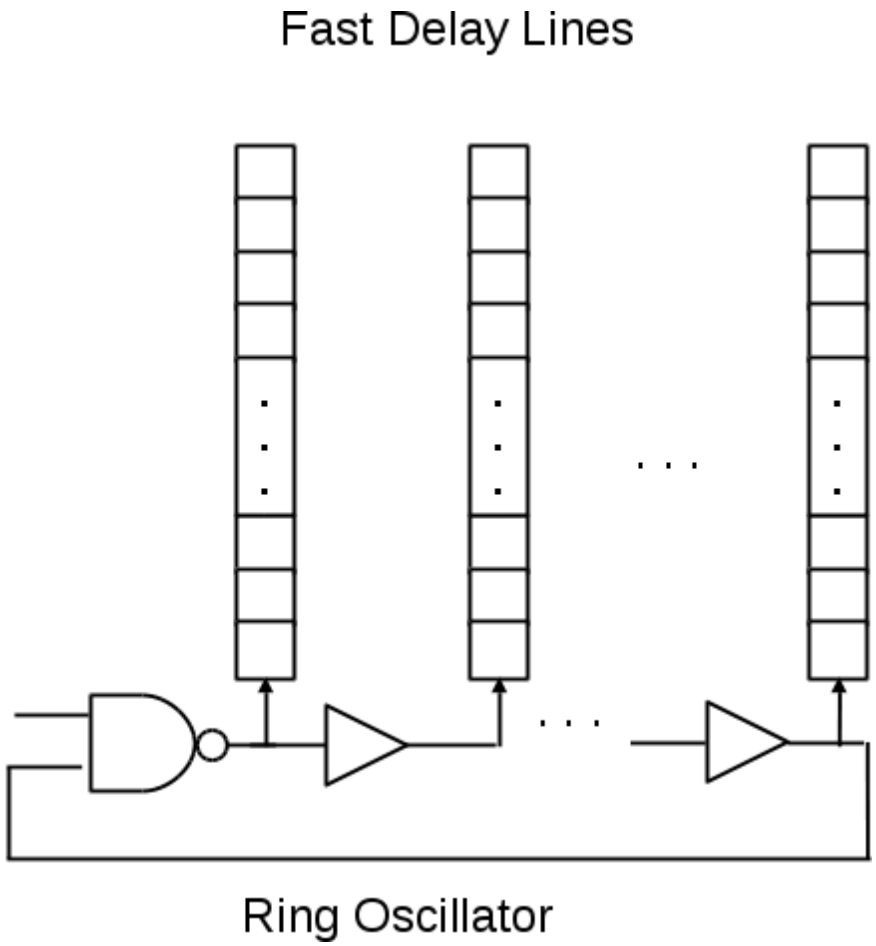
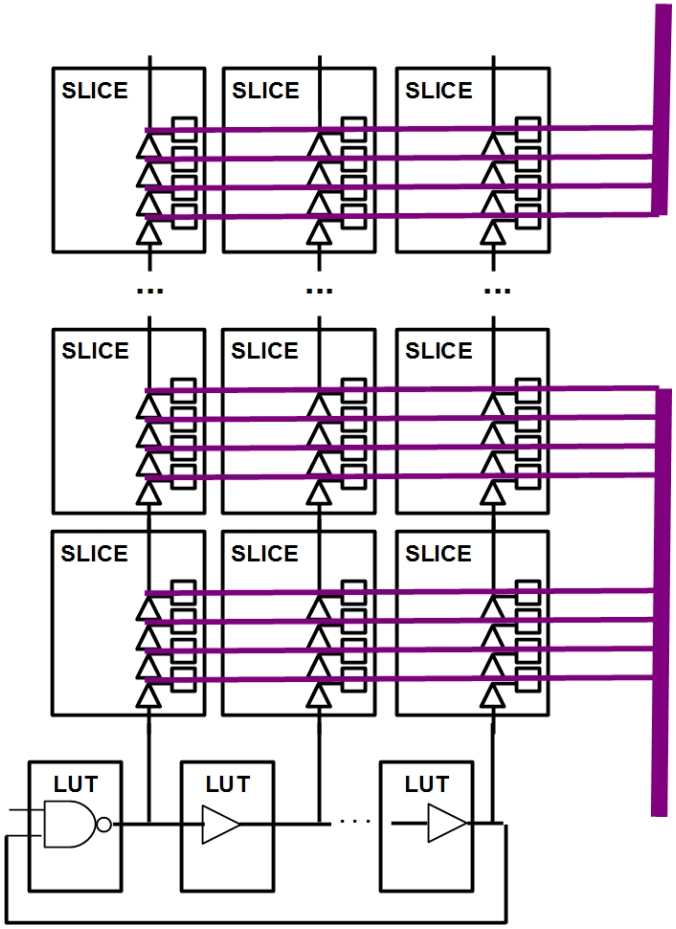
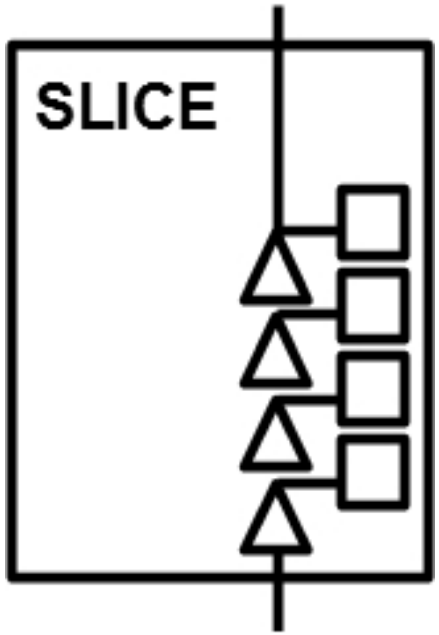
Design Parameters



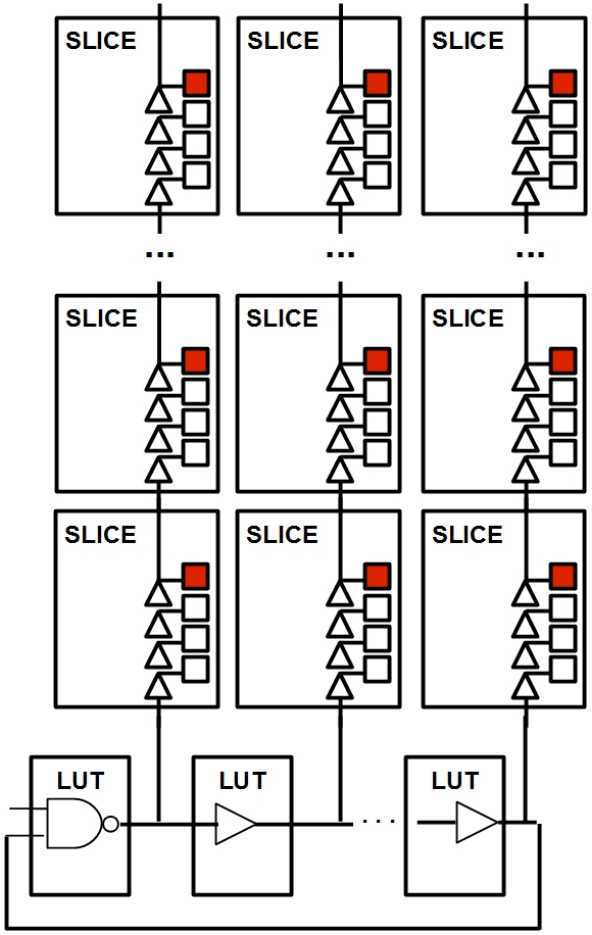
- n=3
- m=36
- t=N*10ns

Non-Linearity





Non-Linearity – Downsampling



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Results

Na	k	H	n_{pf}	Throughput1 [Mbps]	H_{min}	Throughput2 [Mbps]
1	1	0.917	3	33.33	0.58	28
2	1	0.994	2	25	0.88	22
3	1	0.999	1	33.33	0.96	16
5	4	0.42	15	1.33	0.13	1.3
10	4	0.77	5	2	0.36	1.82
15	4	0.9	3	2.22	0.55	1.83
20	4	0.95	2	2.5	0.68	1.7
25	4	0.98	2	2	0.78	1.56

Results - resources

k	Platform	Resources
1	Spartan6	64 slices
4	Spartan6	40 slices

Conclusions and Future Work

- Carry-chain primitives provide high-precision measurements of accumulated jitter
- Highly efficient entropy extraction on FPGAs
- High throughput (>MHz) with low resources (<70 slices)
- Future work
  - Improve arithmetic post-processing
  - Modify stochastic model to account for non-linearities
  - On-the-fly testing

Thank You

Questions? Comments?

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