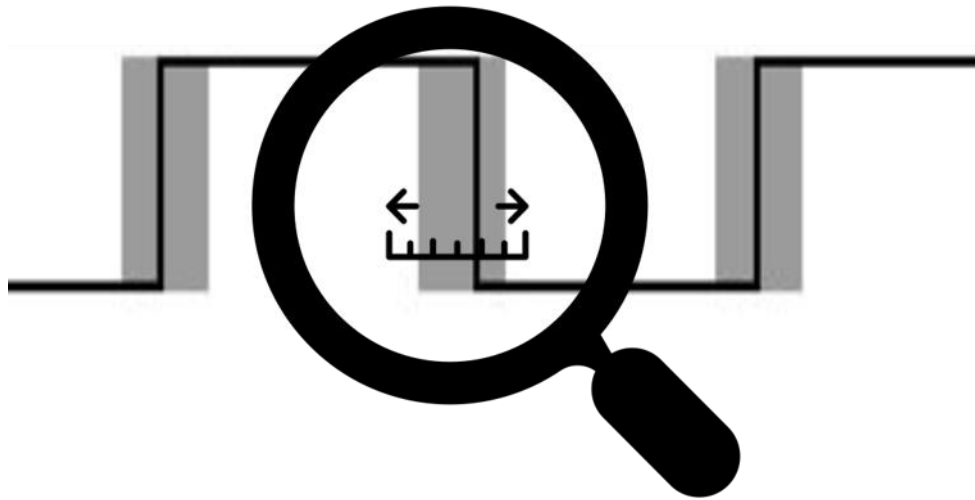




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# An evaluation procedure for comparing clock jitter measurement methods

Arturo Mollinedo Garay

Florent Bernard

Viktor Fischer

Patrick Haddad

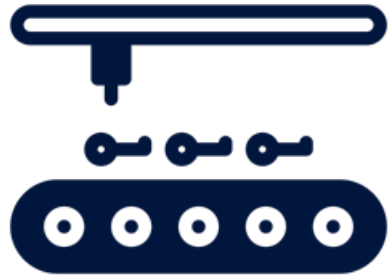
Ugo Mureddu



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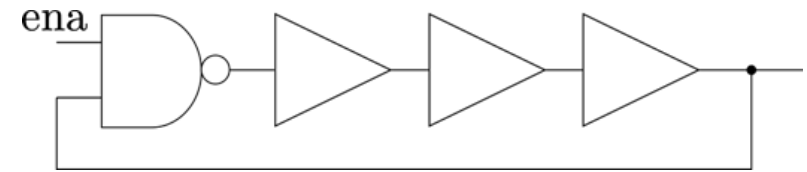
# Brief reminder – clock jitter



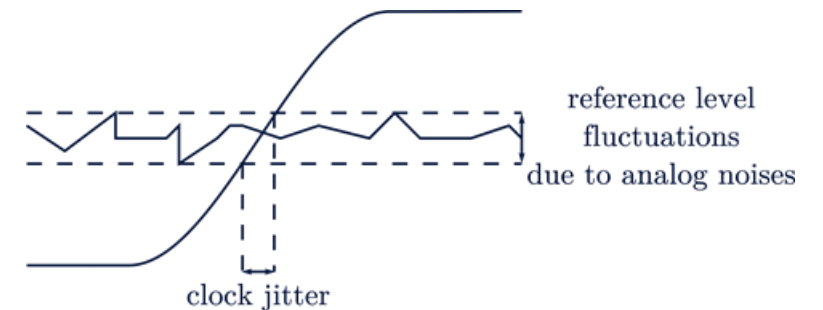
TRNGs are used to generate the inputs of cryptographic systems



A randomness source is required

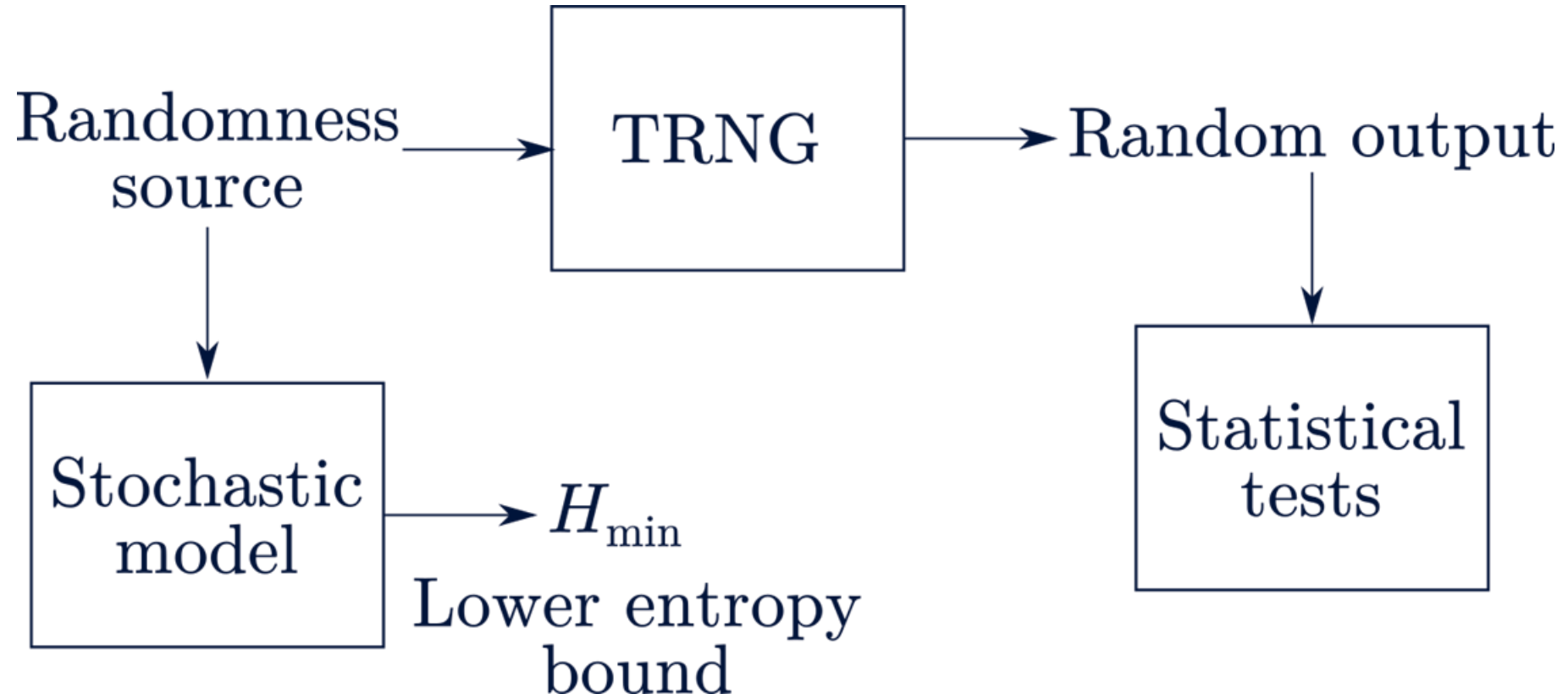


Ring oscillators are easily implementable in digital circuits

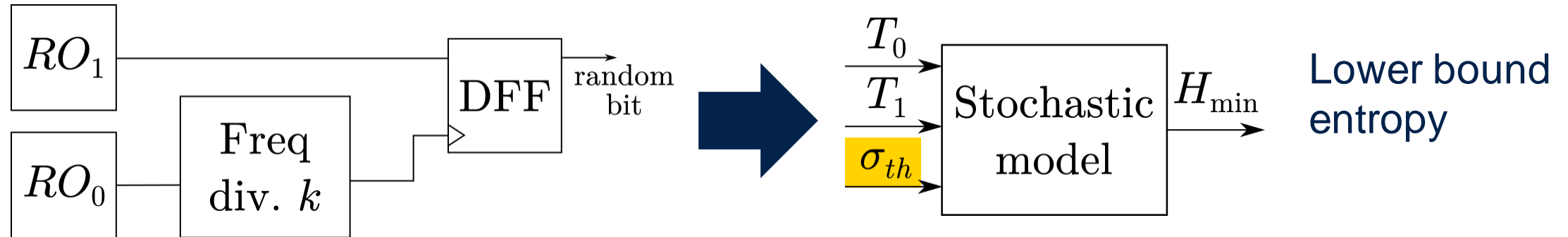


These fluctuations are an inevitable phenomena

# Evaluation of a TRNG



# eRO-TRNG



eRO-TRNG

Online and embedded  
measurement of  $\sigma_{th}$

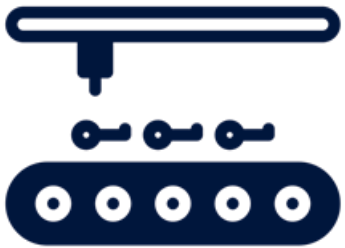
Guarantee of the  
TRNG performance



# The final goal



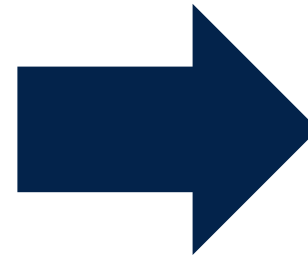
The need for true random numbers



eRO-TRNGs use jittery digital signals



Embedded and continuous measurements are required for the entropy source characterization and for its performance evaluation.



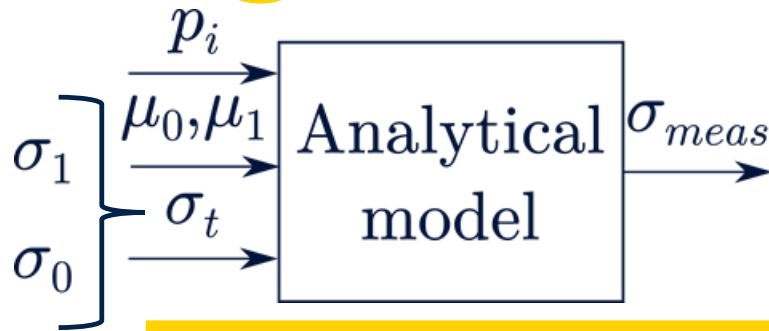
**Thoroughly evaluate jitter measurement methods**

# The evaluation procedure

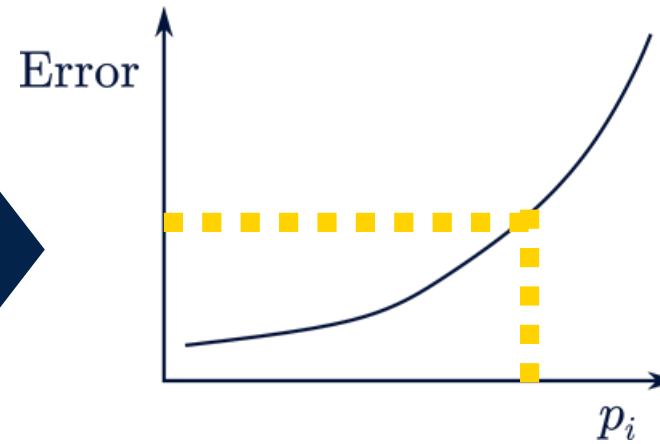


# The evaluation procedure

## 1 Modeling



Neglect flicker noise  
Clock jitter  $\sigma = 1\text{‰}\mu$   
 $T \sim \mathcal{N}(\mu, \sigma^2)$



## 2 Simulation

$$err_{\%} = \frac{|\sigma_t - \sigma_{meas}|}{\sigma_t} \cdot 100$$

## 3 Error analysis

Maximal error < 25%.  
Average error < 10%.

Methods constraints on  $P_i$

## 4 Hardware experiment



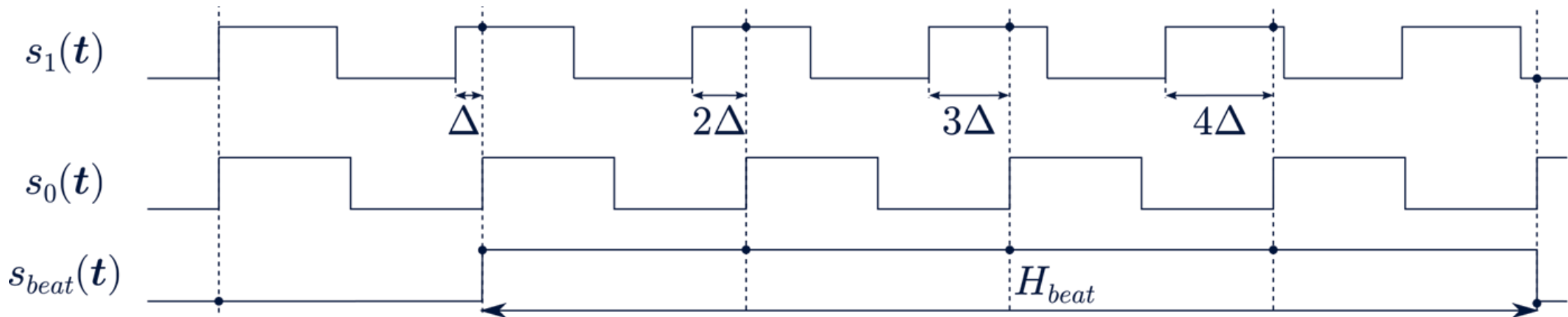
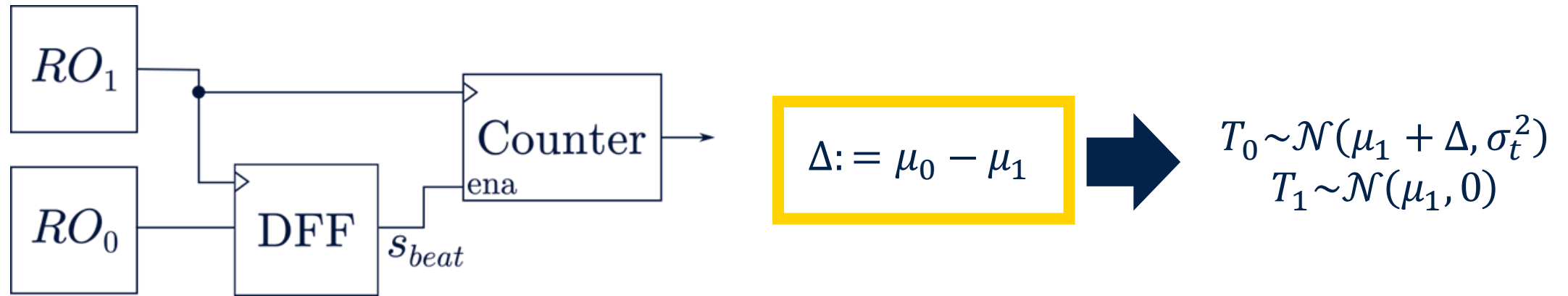
# STEP 1 – Analytical model





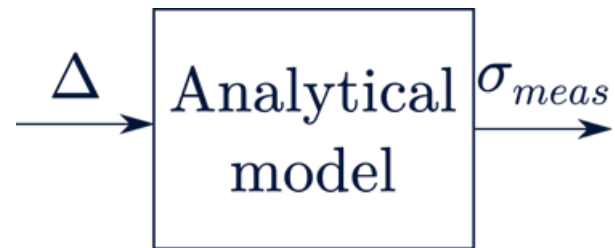
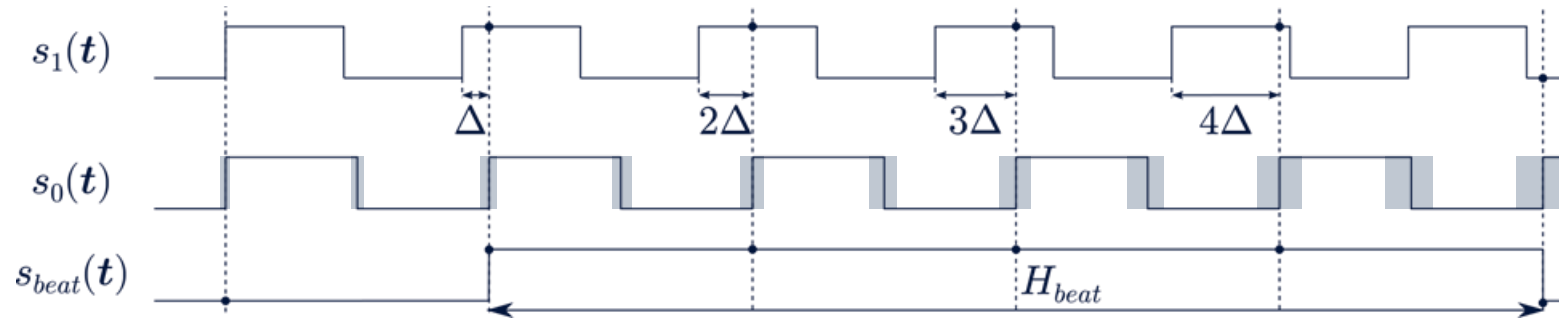


# The coherent sampling method





# On the analytical model



## The precision of the method

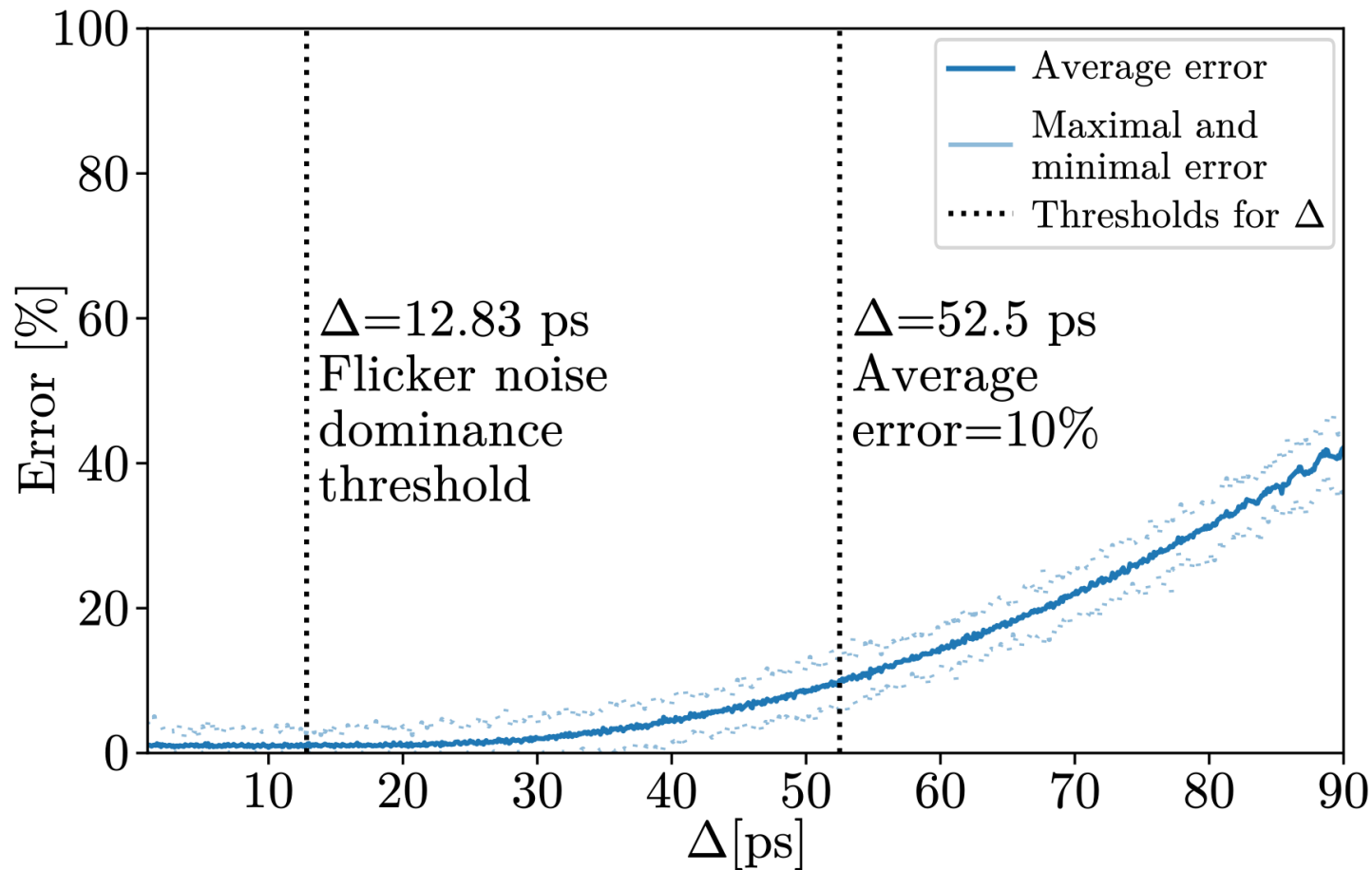
- Jitter accumulates with time
- Precision of the method depends on  $\Delta$ .
- We control  $\Delta$  on simulations.

## STEP 2 – Simulations





# The coherent sampling method



- Analyse  $err_{\%} = f_{\sigma_{inp}}(\Delta)$
- Lower limit  $\rightarrow$  flicker noise influence [3]
- Upper limit  $\rightarrow$  acceptance limit on the error.

## STEP 3 – Study the results





# The coherent sampling method

The interval can be found for any  $\mu_1$

- If  $\Delta$ :

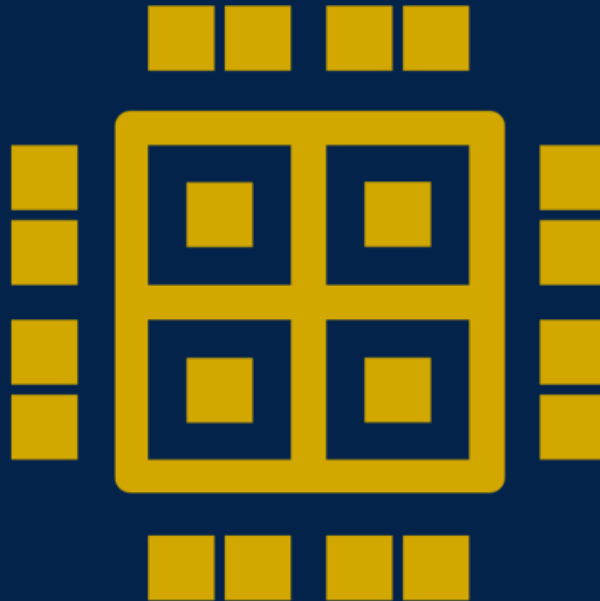
$$\Delta_{i,j} = \frac{|\mu_i - \mu_j|}{\mu_j} 100\% ; i \neq j$$

$\mu_j \rightarrow$  sampled clock ;  $\mu_i \rightarrow$  sampling clock

- Then:

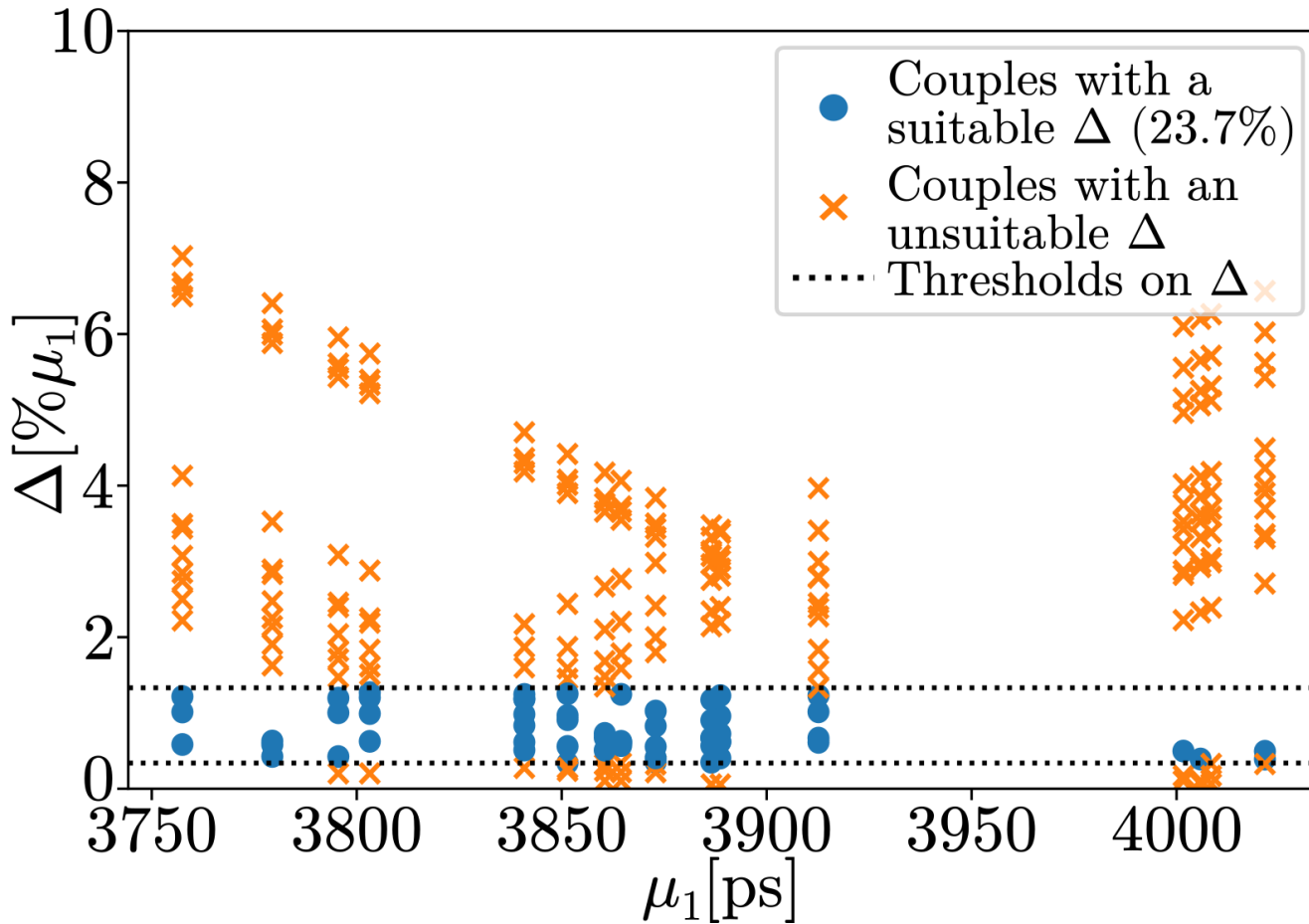
$$0.3\% \mu_1 < \Delta < 1.4\% \mu_1$$

# STEP 4 – Hardware experiment





# The coherent sampling method



- 16 ROs  $\rightarrow$  240 pairs of ROs
- 23.7% had a suitable  $\Delta$ .
- The critical dependence on  $\Delta$  makes the method difficult to implement in hardware



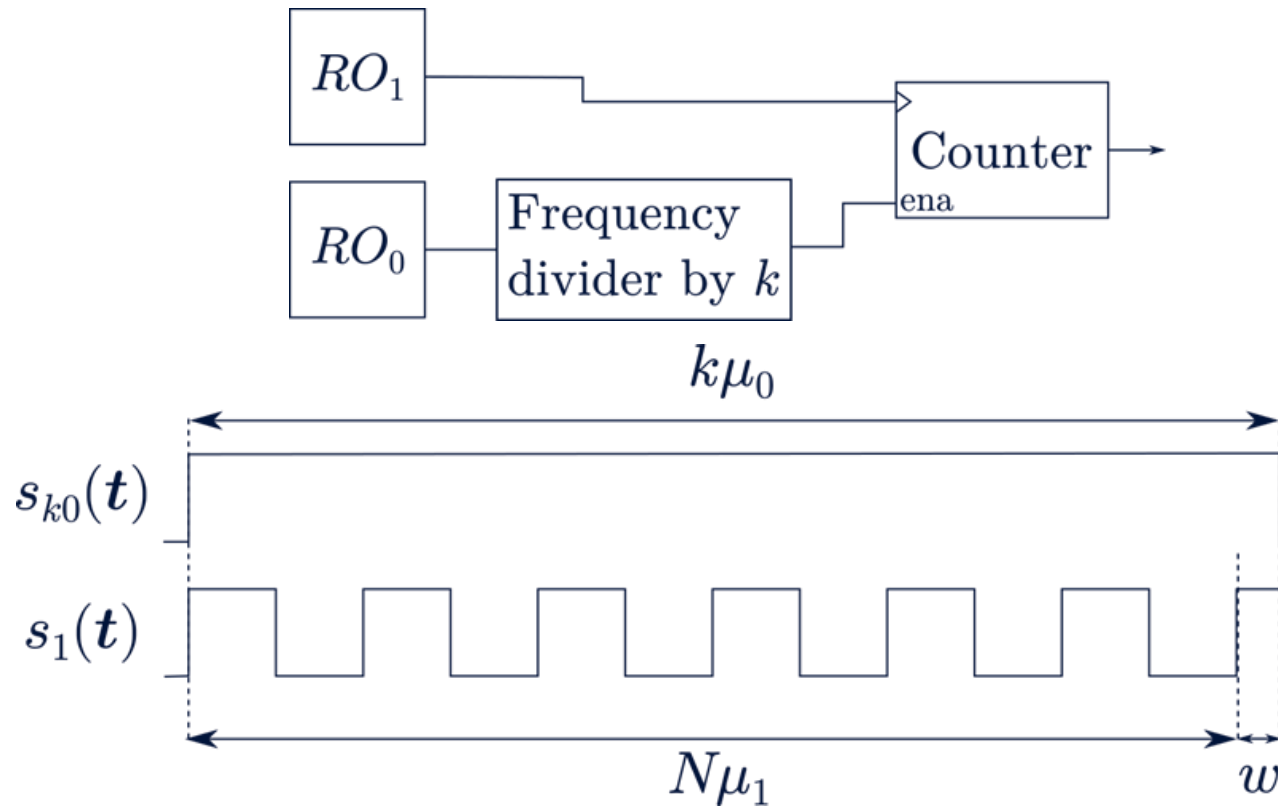
# Application of the procedure





# The counter method

The variance of the counter values is used to calculate the jitter after the accumulation time  $k\mu_0$  [4]

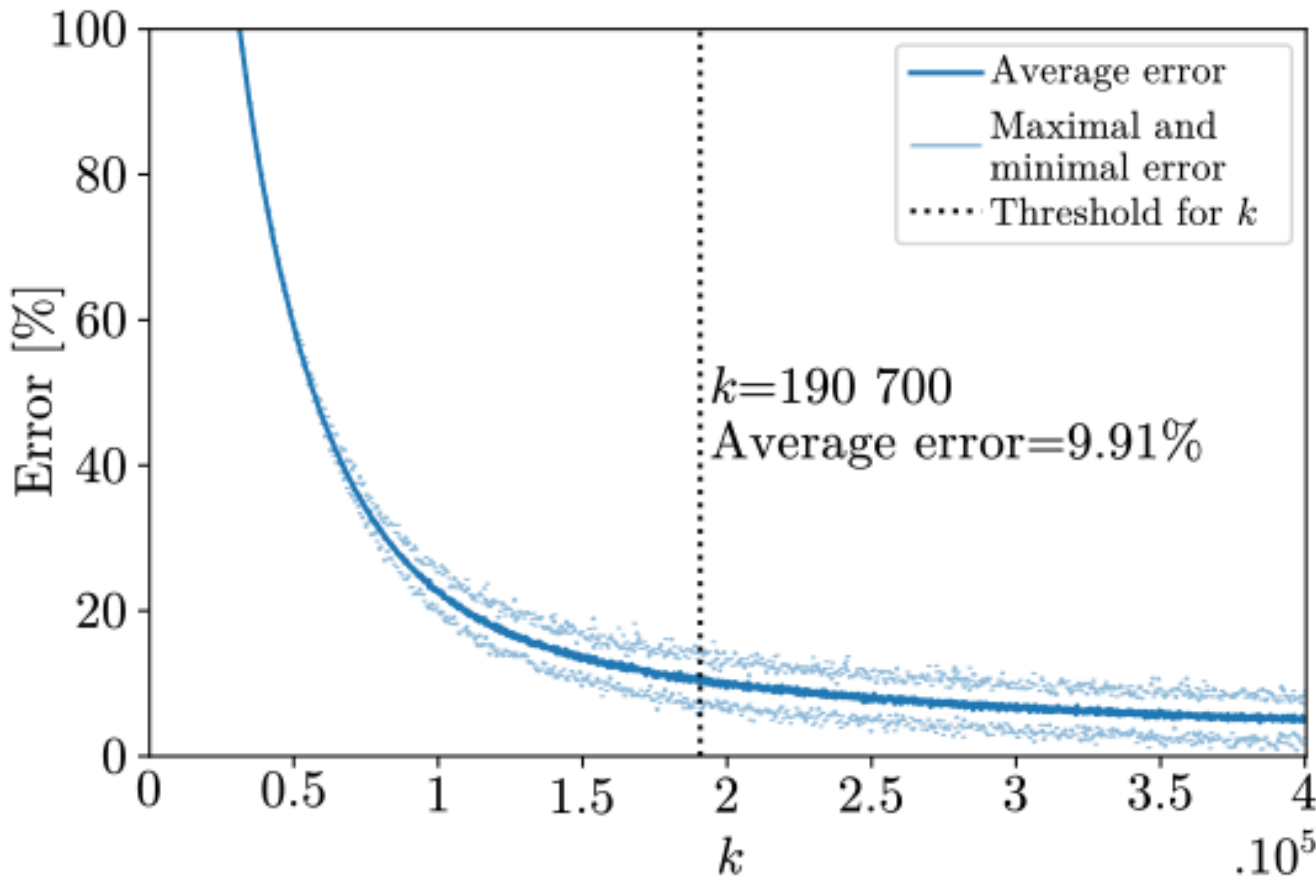


- The precision depends on  $k$
- $k$  chosen by the designer
- No hardware constraint

[4] Valtchanov, B., A. Aubert, F. Bernard, and V. Fischer. "Modeling and Observing the Jitter in Ring Oscillators Implemented in FPGAs." In Proceedings of the 11th IEEE Workshop on Design & Diagnostics of Electronic Circuits & Systems - DDECS 2008, 158–63, 2008.



# The counter method

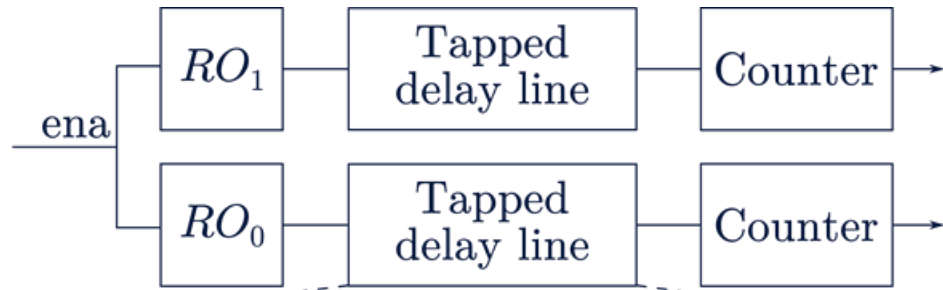


- Acceptable error for  $k > 200,000$
- Flicker noise is not negligible for  $k > 300$  [3]
- The method does not distinguish between the thermal noise and the flicker noise components
- The counter method is not applicable for thermal noise clock jitter measurement.

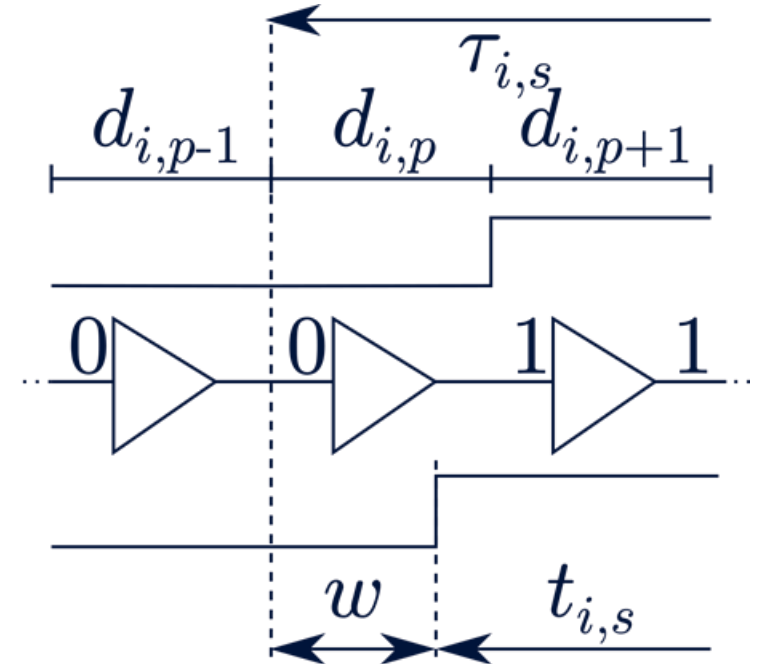
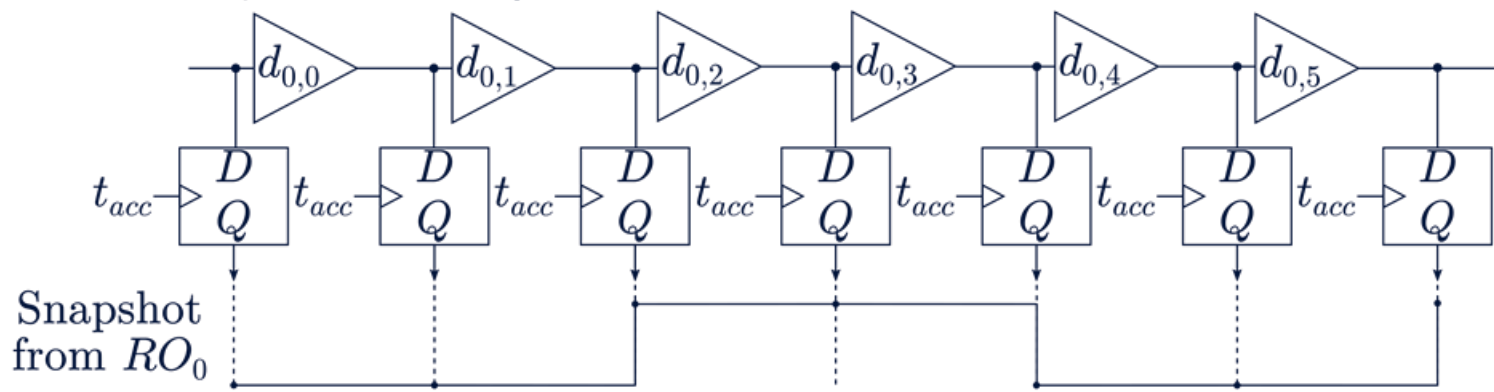


# The differential delay line method

The time of arrival of two edges coming from two ROs are measured with two delay lines [5]



Tapped delay line for  $RO_0$





# The differential delay line method

## Simulations

- The delays of the buffers are given by the hardware.
- Variations in manufacturing → not identical delays.

$$d_{i,j} \sim \mathcal{N}(\mu_d, \sigma_d^2)$$

- Results

$$\mu_d < 18ps ; \sigma_d < 16.5ps$$

## Hardware experiment

- Results

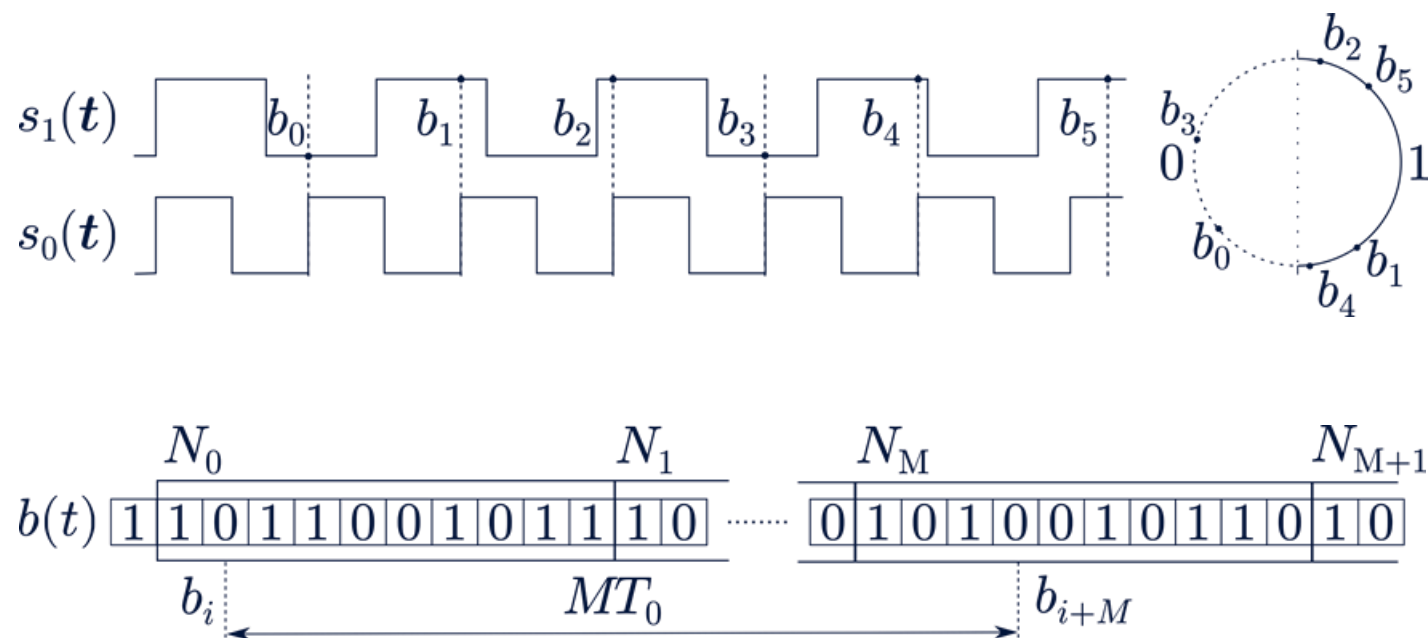
$$\mu_d = 4.84ps ; \sigma_d = 4.26ps$$

- At least 1.5 clock periods → 1,000 buffers ;  $f_0$  of 400MHz.
- Delicate trade-off → cannot be met in the FPGA.



# Method testing the autocorrelation of distant samples

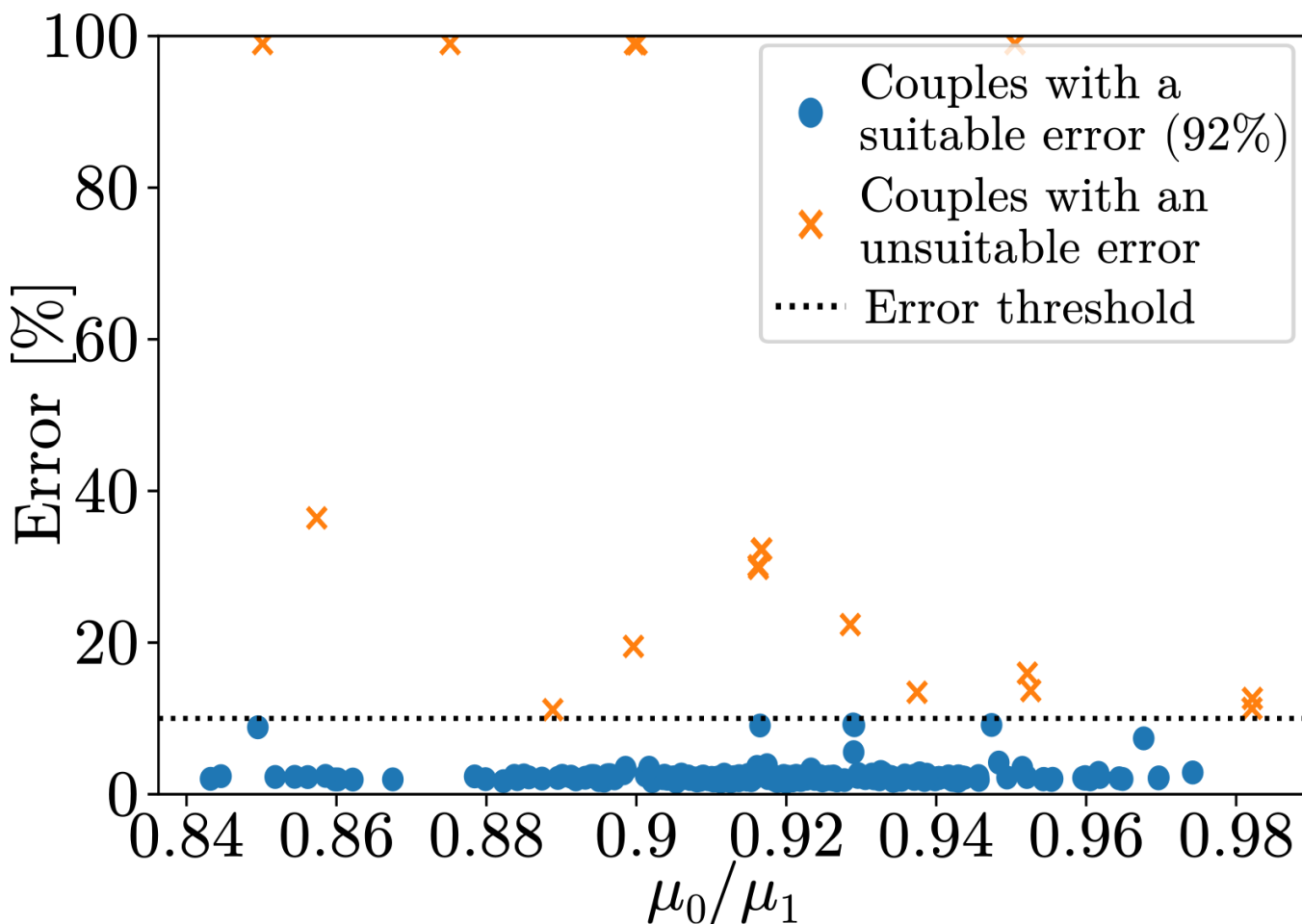
The method is based on the autocorrelation of coherent samples distant in time of a short accumulation time [6]



- Coherent sampling based
- No constraints on  $\Delta$ .
- $\mu_0/\mu_1 \approx p/q$ ;  $p, q$  small integers.
- Another pattern distant in time of  $M\mu_0 \rightarrow$  accumulated jitter  $M\mu_0$ .



# Method testing the autocorrelation of distant samples



- Group A → 16 ROs, 9 buffers
- Group B → 16 ROs, 10 buffers
- 255 pairs of ROs → sampling from group A ; sampled group B
- 92% resulted in an acceptable error

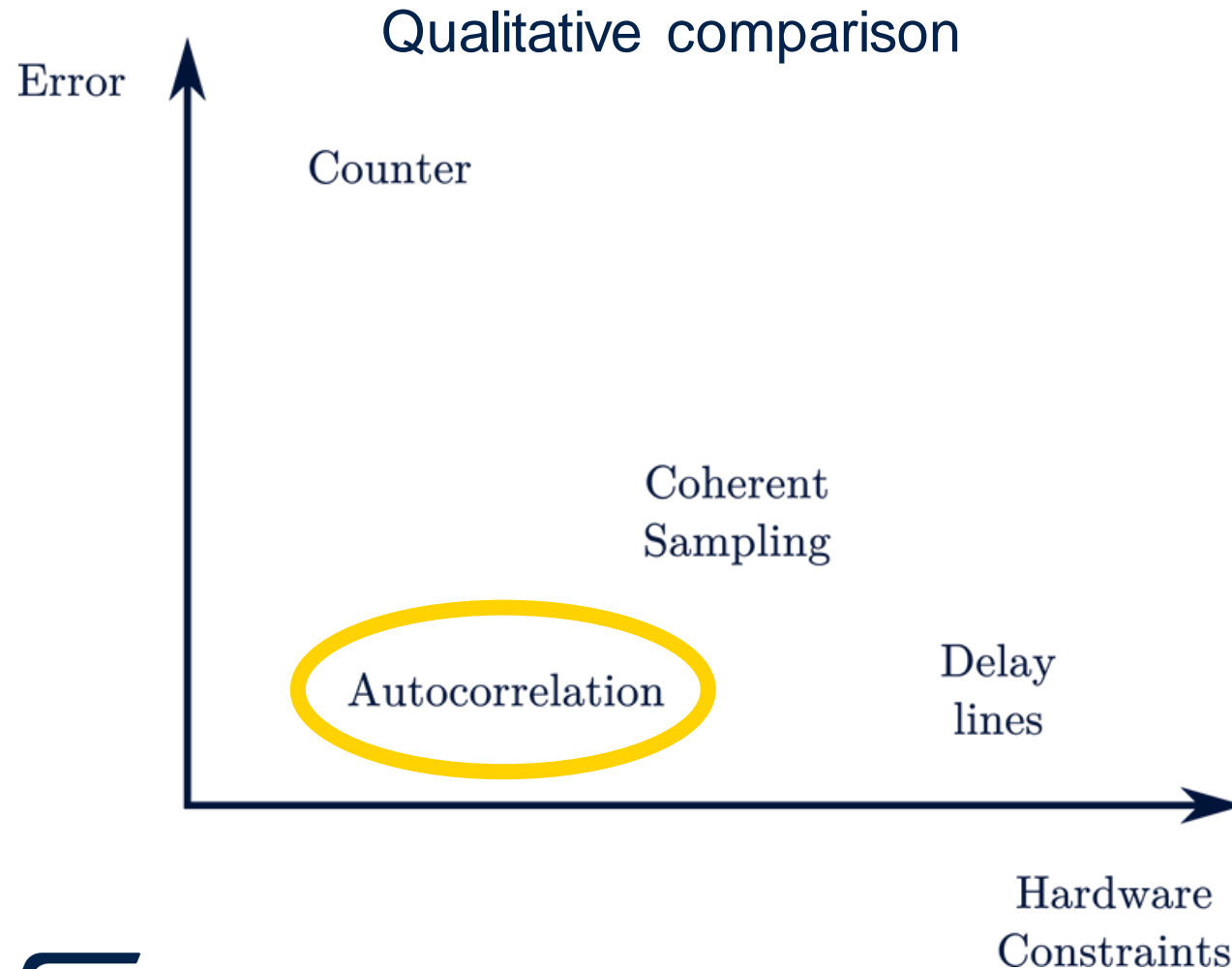
# Results and conclusion







# Results summary



- The method testing autocorrelation of distant samples is ahead of the others
- The rest of them should either:
  - Include the influence of flicker noise in their original model
  - Avoid the influence of flicker noise
  - Relax hardware constraints



# Conclusion

Successfully identified the limits of each method

The models are simplistic compared to reality → inaccurate simulated measurements, inaccurate measurements in hardware

Accurate simulated measurements DO NOT mean accurate measurements in hardware

Our evaluation procedure is necessary but not sufficient

# Our technology starts with You



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