LABORATOIRE HUBERT CURIEN

UMR • CNRS • 5516 • SAINT-ETIENNE

Asynchronous S-Boxes: Designing Clockless First-Order Masked Functions

Mateus Simões

Agenda

1 Introduction

2 Self-Timed Masking

3 Implementation Results

4 Conclusion

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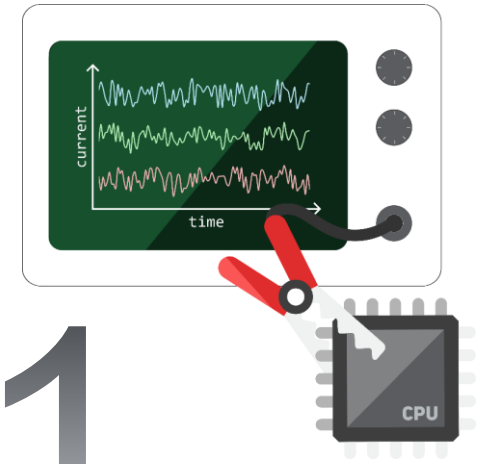
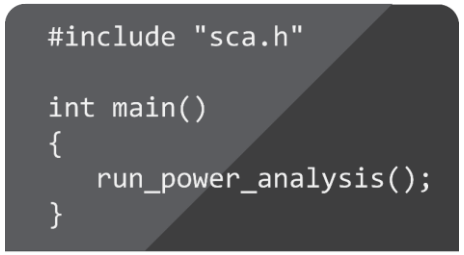
Side-Channel Attacks (SCA) [KJJ99]



1

The attacker measures the device's power consumption during the encryption

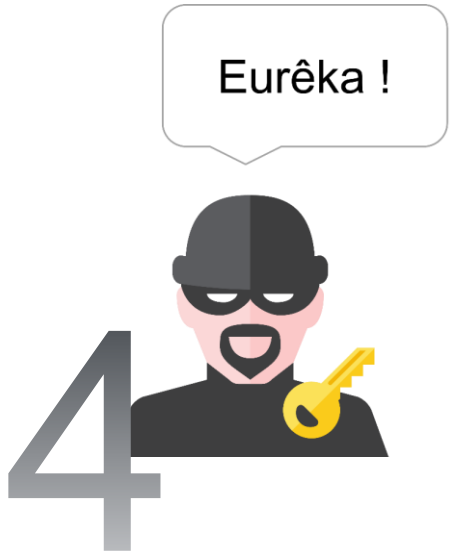


2

From the acquired data, the attacker performs several side-channel analysis.

3

The analysis rank all possible key hypothesis, in order to find the secret key.



4

If the analysis is successful, the attacker has therefore access to the encrypted data.

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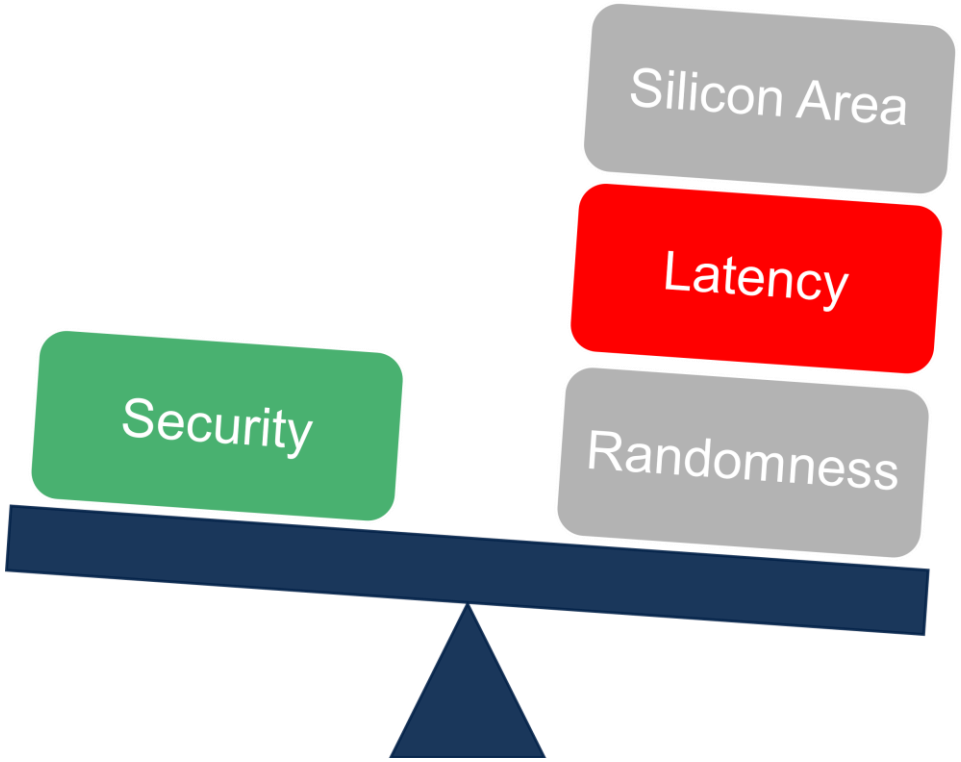
d-Order Boolean Masking [GP99]

A secret Boolean variable x is split into $d + 1$ shares x_i:

$$x = x_0 \oplus x_1 \oplus \cdots \oplus x_d.$$

The side-channel behavior depends on the random shares of x, not on x itself.



Objectives

1	Replace registers with asynchronous latches in order to obtain self-timed masking schemes.
2	Evaluate the performance of secure masked schemes operating as self-timed circuits.
3	Evaluate the importance of fresh randomness in self-timed masked implementations.

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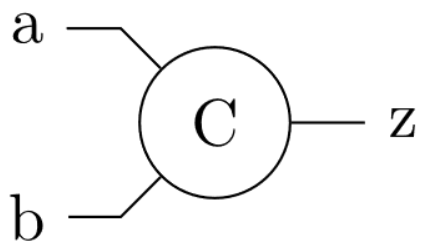
Self-Timed Masking

Self-Timed Latches [MB59]

Built upon Muller c-elements [MB59].



a	b	z_{n+1}
0	0	**0**
0	1	z_n
1	0	z_n
1	1	**1**

Figure: A Muller c-element's symbol and its truth table.

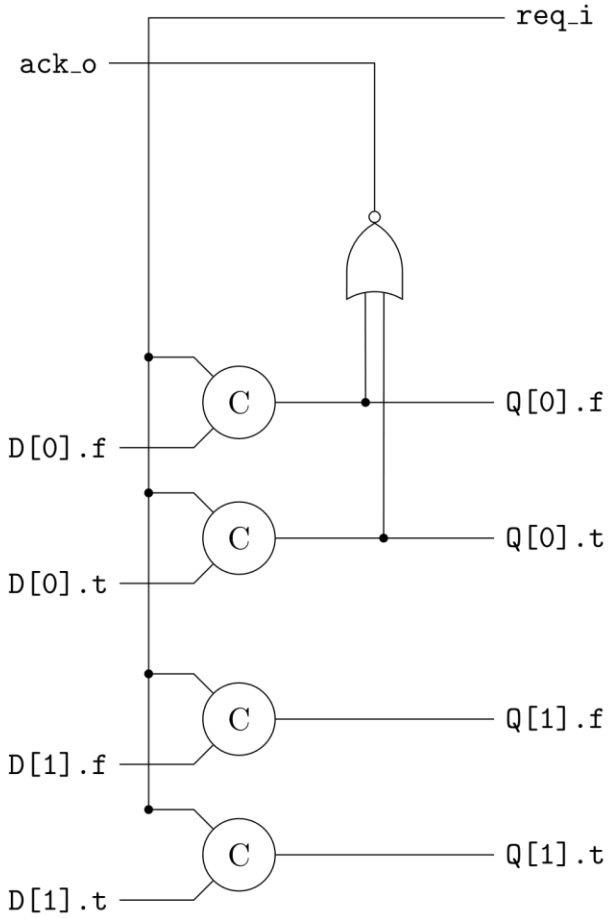


Figure: The self-timed latch.

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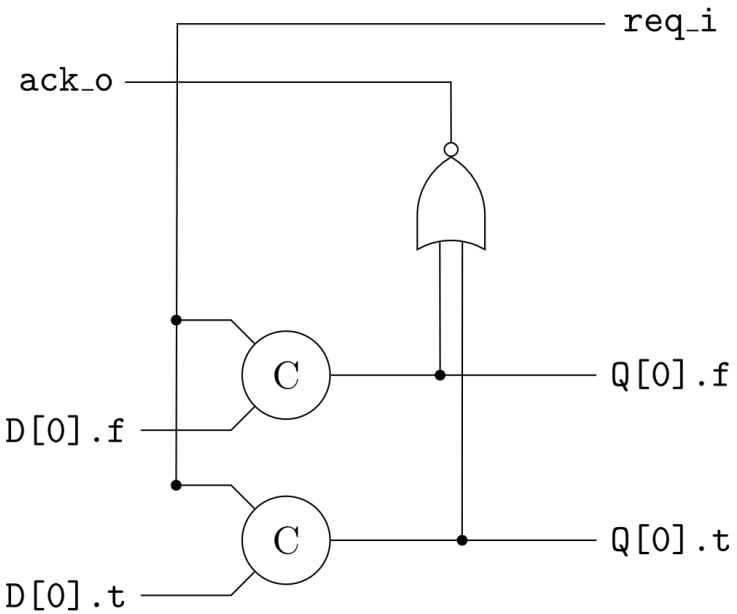
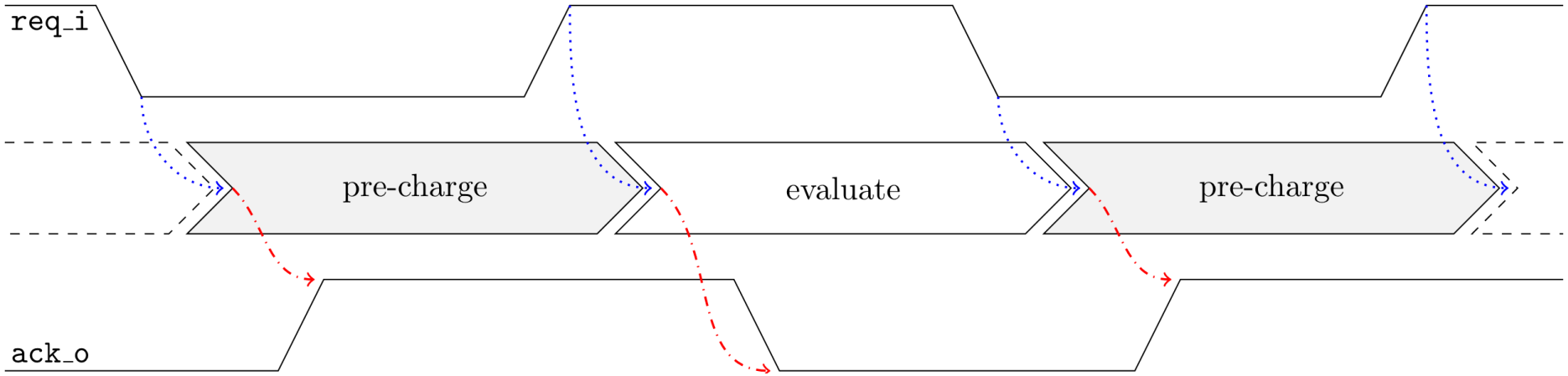
Dual-Rail Protocol with Pre-Charge / Evaluate Logic

Encodes a bit using two signals [DN95].

Token x	x.t	x.f
Null (Ø)	0	0
0	0	1
1	1	0
Not Used	1	1





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The Danger of Glitches

A glitchy function may leak the secret variable [MPG05, MPO05].

$$f_0(x_0, y_0, y_1) = x_0 y_0 \oplus x_0 y_1 \rightarrow \text{⚡} \rightarrow x_0 \oplus y$$

f_0 depends on the secret y

Let us suppose a signal b is faster than a:

Input Transition		Dual-Rail Function		
$a_I \rightarrow a_F$	$b_I \rightarrow b_F$		$z = a\ AND\ b$	$z = a\ XOR\ b$
$1 \rightarrow 0$	$0 \rightarrow 1$	z.t	$0 \rightarrow 1 \rightarrow 0$ ⚠	$1 \rightarrow 0 \rightarrow 1$ ⚠
$1 \rightarrow 0$	$1 \rightarrow 0$		$1 \rightarrow 0$	$0 \rightarrow 1 \rightarrow 0$ ⚠

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Avoiding Glitches [Juk21]

Dual-Rail Functions

a	b	z
∅	∅	∅
∅	valid	∅
valid	∅	∅
valid	valid	valid

Pre-Charge / Evaluate Logic

+

Dual-Rail Monotonic Functions

No Glitches

Stage	Input Transition		Dual-Rail Function	
	$a_I \rightarrow a_F$	$b_I \rightarrow b_F$	$z = a\ AND\ b$	$z = a\ XOR\ b$
Pre-Charge	$1 \rightarrow \emptyset$	$0 \rightarrow \emptyset$	$0 \rightarrow \emptyset$	$1 \rightarrow \emptyset$
	$1 \rightarrow \emptyset$	$1 \rightarrow \emptyset$	$1 \rightarrow \emptyset$	$0 \rightarrow \emptyset$
Evaluate	$\emptyset \rightarrow 1$	$\emptyset \rightarrow 1$	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 0$
	$\emptyset \rightarrow 1$	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 1$

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Single-Cycle Processing

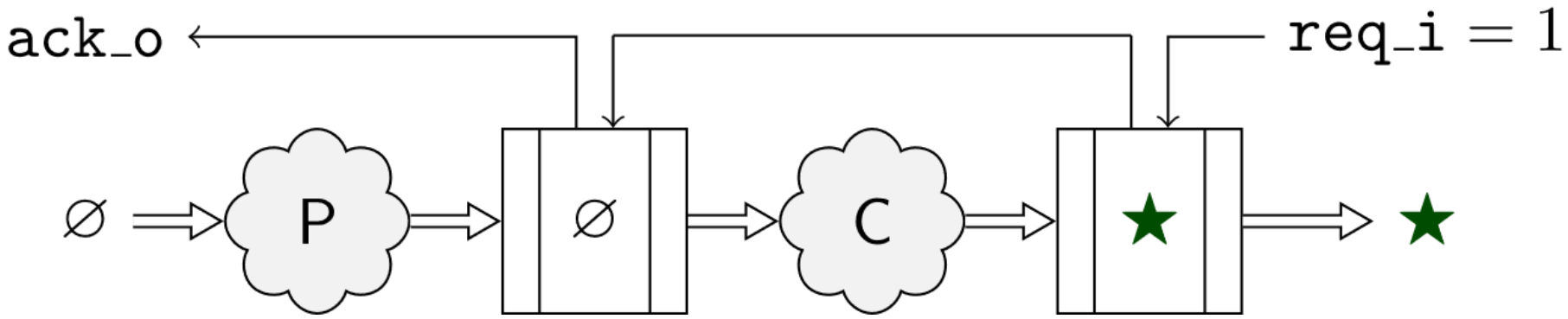
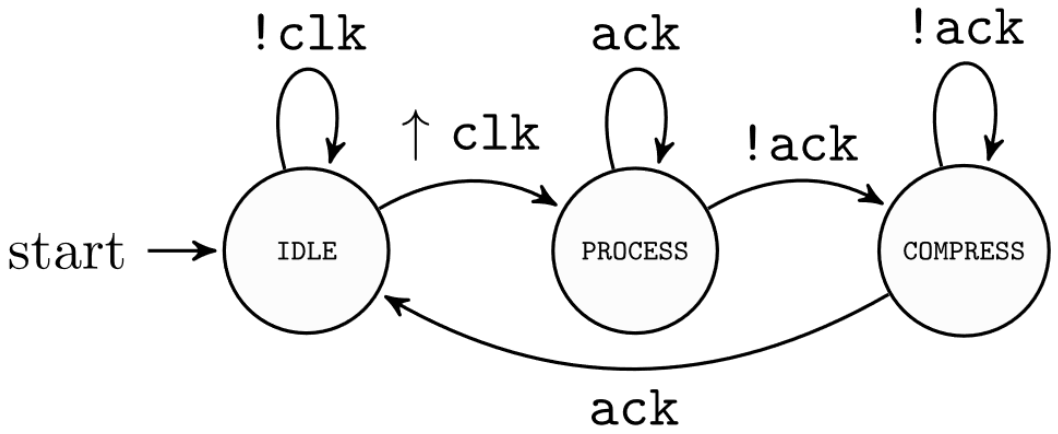


Figure: The self-timed PRESENT S-box.



State	S-box Inputs	
	token	req_i
IDLE	∅	1
PROCESS	⋆	0
COMPRESS	∅	1

Self-Timed Gadgets

Replacing Registers with Self-Timed Latches

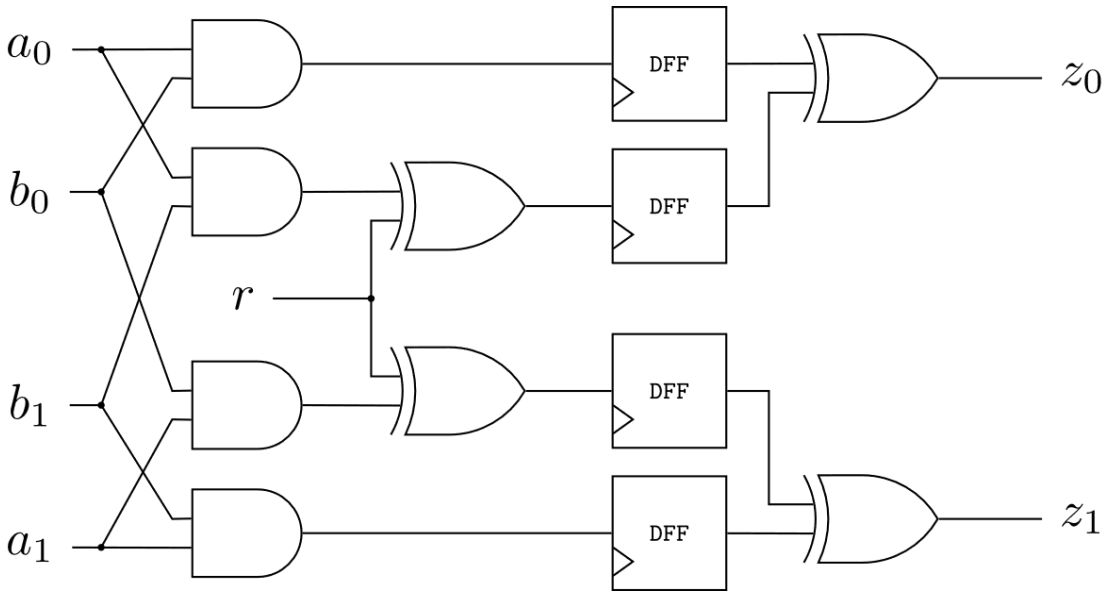


Figure: Original DOM Gadget [GMK16].

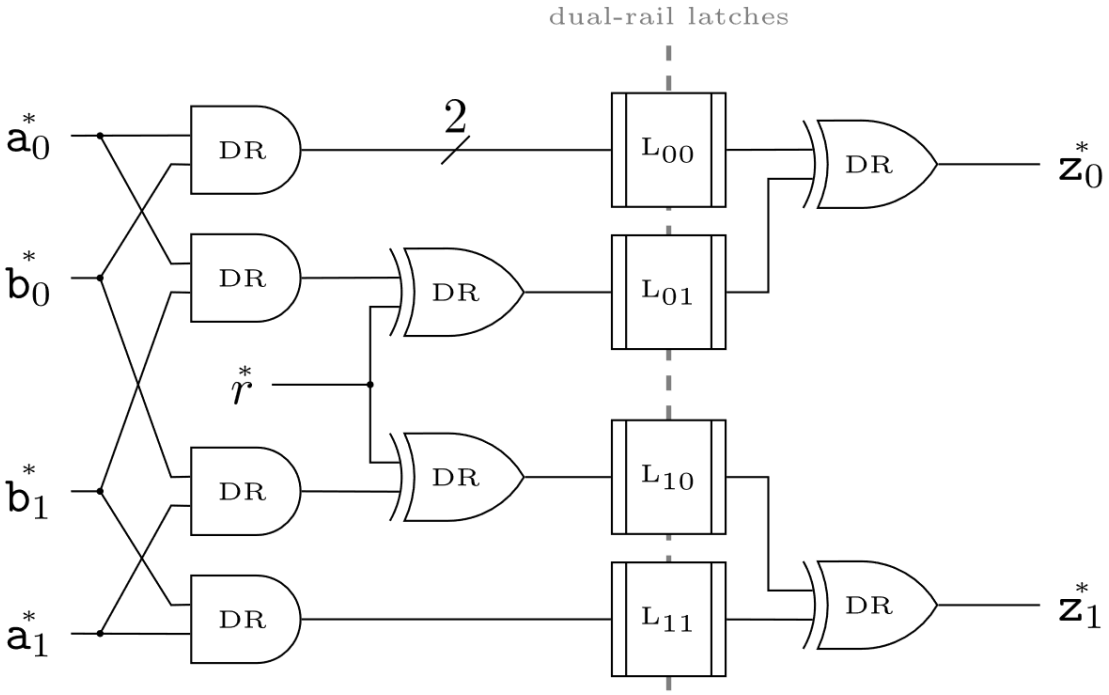


Figure: Self-Timed DOM Gadget.

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Randomness *vs* Self-Timed Masking

Data dependent evaluation time may be a threat to self-timed circuits.

Does the self-timed feature guarantee first-order masking security?

S-boxes without random refresh bits	S-boxes with random refresh bits
❑PRESENT [SM21] ❑AES [SM21]	❑TI PRESENT ❑DOM AES [GMK16]

Implementation Results

Implementation Results | PRESENT and AES S-boxes

Design	Shares	Area [1] [kGE]	Refresh [bits]	Latency [cycles]	Standard Cell Library
PRESENT [PMK+11]	3	0.36	0	1	UCM 180-nm
PRESENT [this work]	**2**	**0.99**	**0**	**1**	**STM 40-nm**
PRESENT [this work]	**2**	**1.02**	**8**	**1**	**STM 40-nm**
AES [UHA17]	2	1.40	64	5	TMSC 65-nm
AES [WM18]	4	4.20	0	16	UCM 180-nm
AES [Sug19]	3	3.50	0	4	NanGate 45-nm
AES [GMK16]	2	2.80	28	5	UCM 180-nm
AES [GMK16]	2	2.60	18	8	UCM 180-nm
AES [this work]	**2**	**7.79**	**0**	**1**	**STM 40-nm**
AES [this work]	**2**	**6.07**	**18**	**1**	**STM 40-nm**

[1] ***based on a 2-input NAND gate.***

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Simulating Side-Channel Behavior

- ✓ Test Vector Leakage Assessment (TVLA) [GJJR11]
- ✓ 2 million fixed *vs* random simulated traces
- ✓ Noiseless analysis
- ✓ 1 ps time span

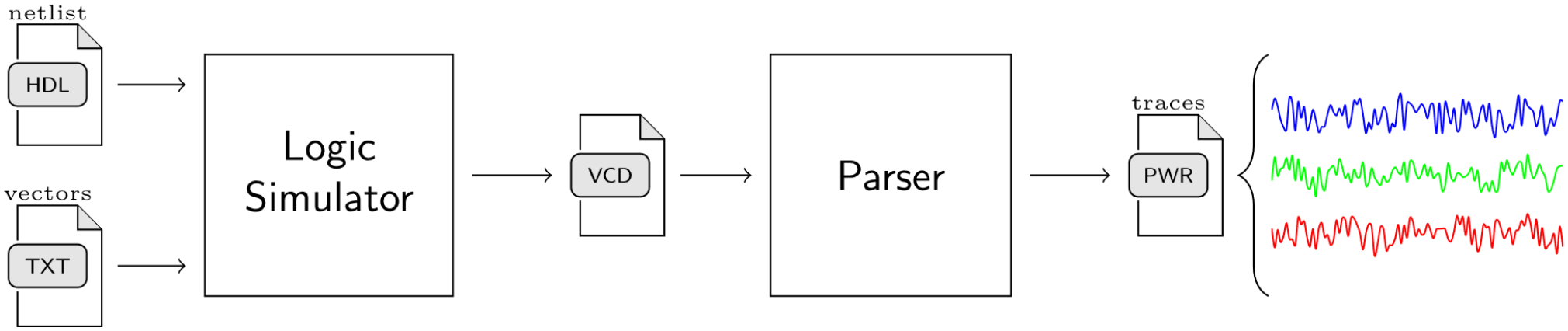

Figure: Modeling the power consumption based on the system's toggling activity.

TVLA: PRESENT S-boxes

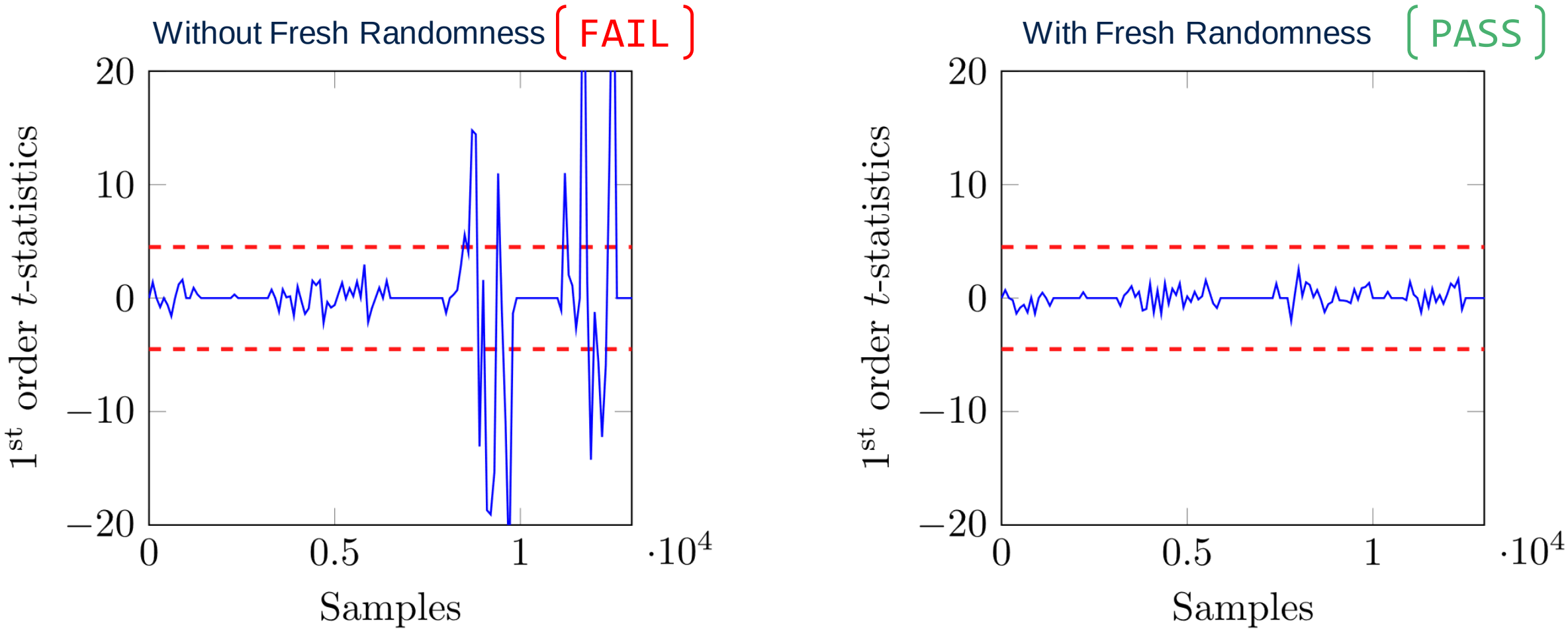

Figure: Based on two million simulated traces.

TVLA: AES S-boxes

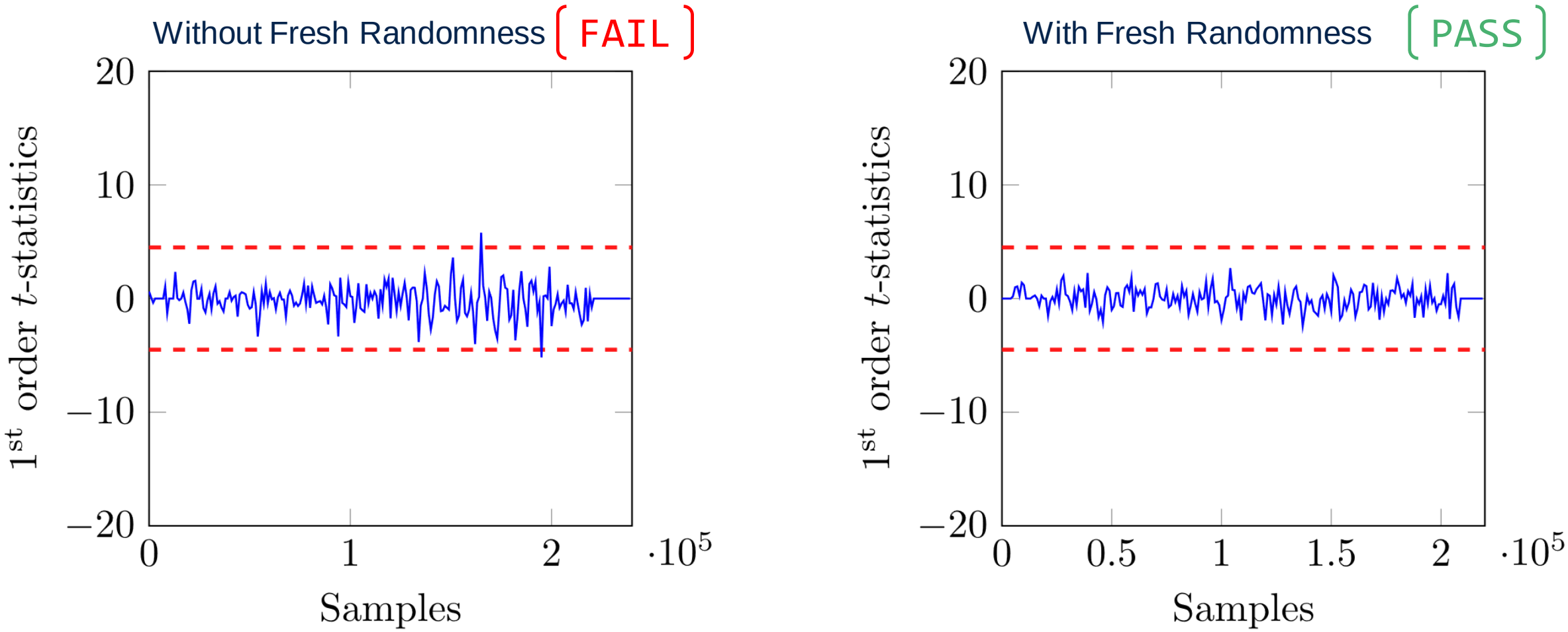

Figure: Based on two million simulated traces.

Conclusion

Conclusion

1. Use of self-timed latches to obtain single-cycle hardware masked S-boxes.
2. Implementation of glitch-free circuits using monotonic logic.
3. How to avoid the early propagation effect in dual-rail gadgets.
4. Locally-asynchronous globally synchronous implementation.
5. Needs fresh randomness in order to be first order secure.

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Possible Future Work

1	Implement self-timed higher-order hardware masked S-boxes.
2	From the self-timed S-boxes, design their respective ciphers.
3	Obtain the performance figures from simulation and FPGA.

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Our technology starts with You

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Self-Timed Latches

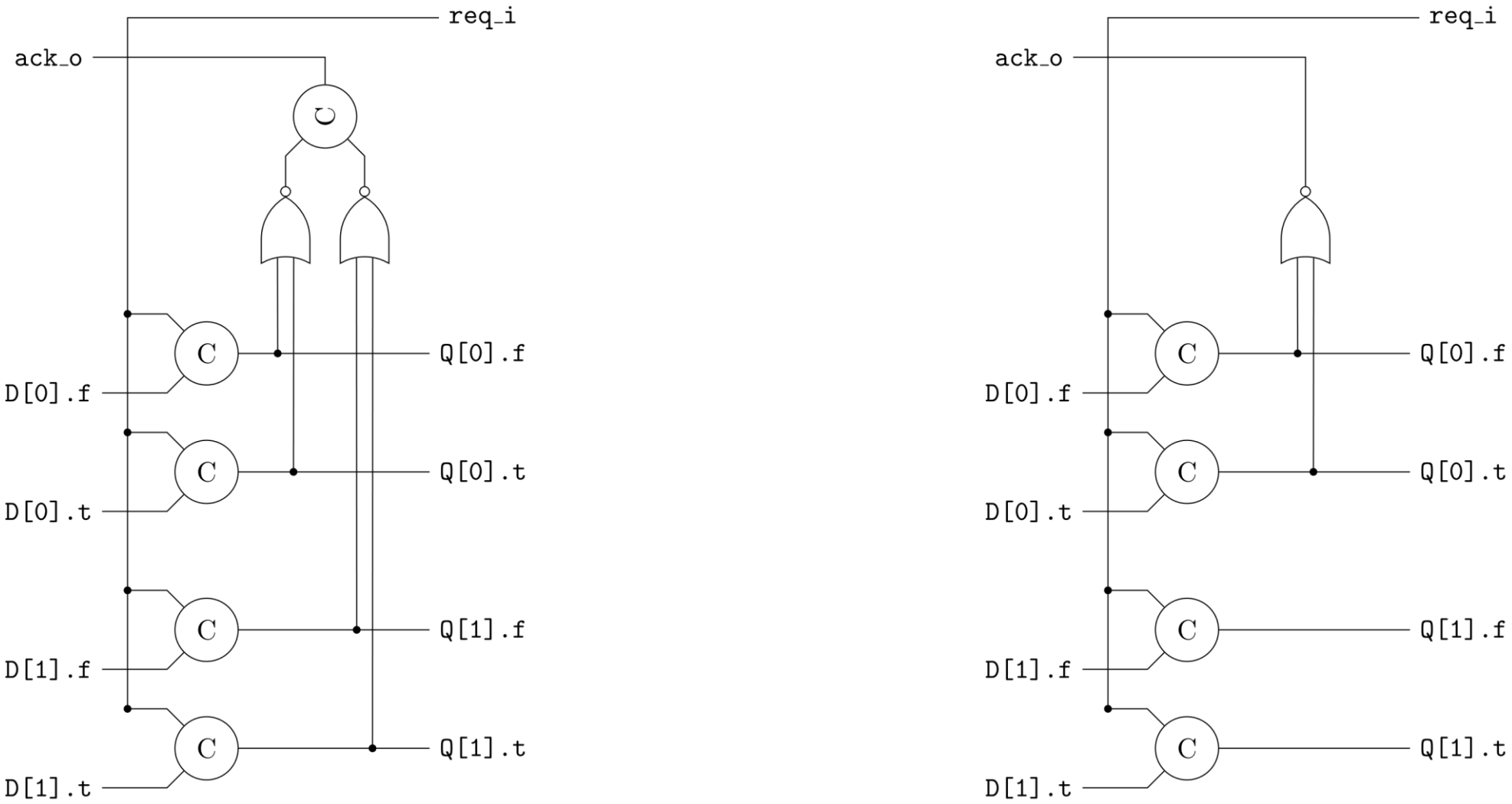
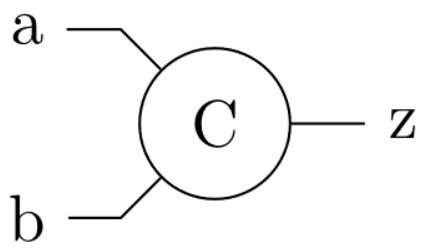


Figure: Strongly indicating (left) and weakly indicating (right) latches.

Muller c-Element [MB59]



a	b	z_{n+1}
0	0	**0**
0	1	z_n
1	0	z_n
1	1	**1**

Figure: The Muller c-element symbol and truth table.

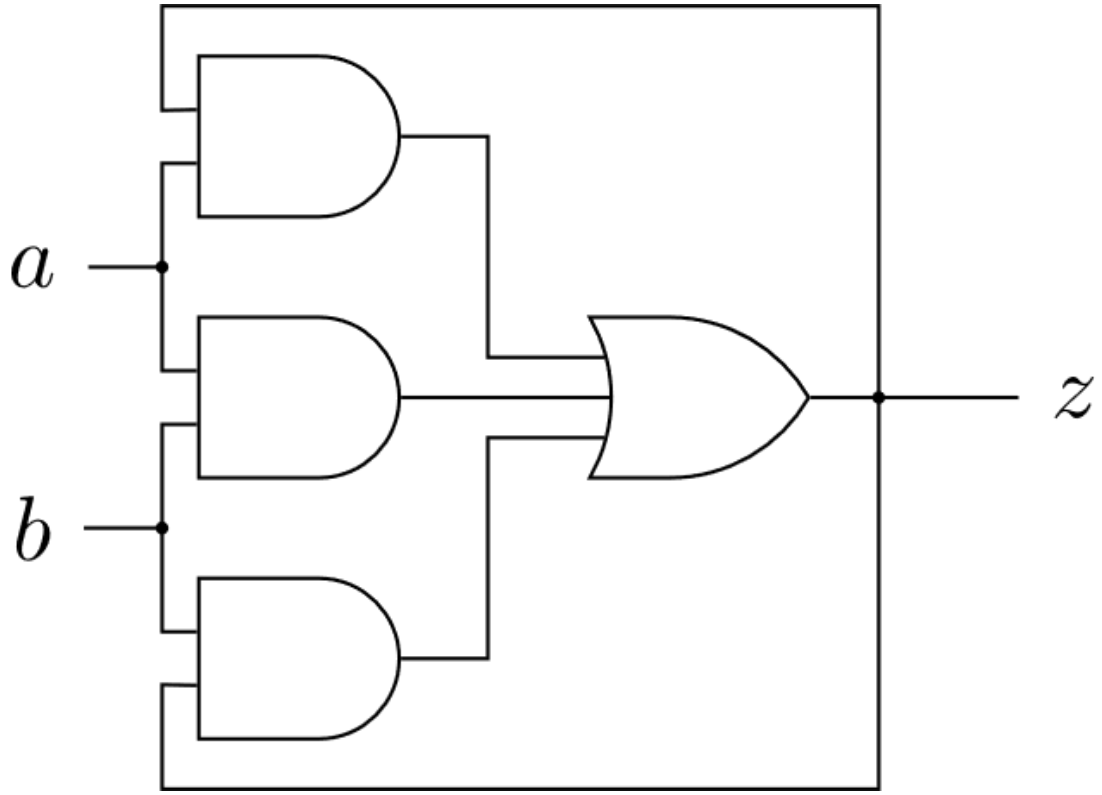


Figure: gate-level implantation.

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The Danger of Glitches

A glitchy function may leak the secret variable [MPG05, MPO05].

$$f_0(x_0, y_0, y_1) = x_0 y_0 \oplus x_0 y_1 \rightarrow \text{⚡} \rightarrow x_0 \oplus y$$

Input Transition		Dual-Rail Function		
$a_I \rightarrow a_F$	$b_I \rightarrow b_F$		$z = a\ AND\ b$	$z = a\ XOR\ b$
$0 \rightarrow 1$	$0 \rightarrow 1$	z.t	$0 \rightarrow 1$	$0 \rightarrow 1 \rightarrow 0$ ⚠
$0 \rightarrow 1$	$1 \rightarrow 0$		0	$1 \rightarrow 0 \rightarrow 1$ ⚠
$1 \rightarrow 0$	$0 \rightarrow 1$		$0 \rightarrow 1 \rightarrow 0$ ⚠	$1 \rightarrow 0 \rightarrow 1$ ⚠
$1 \rightarrow 0$	$1 \rightarrow 0$		$1 \rightarrow 0$	$0 \rightarrow 1 \rightarrow 0$ ⚠
$0 \rightarrow 1$	$0 \rightarrow 1$	z.f	$1 \rightarrow 0$	$1 \rightarrow 0 \rightarrow 1$ ⚠
$0 \rightarrow 1$	$1 \rightarrow 0$		1	$0 \rightarrow 1 \rightarrow 0$ ⚠
$1 \rightarrow 0$	$0 \rightarrow 1$		$1 \rightarrow 0 \rightarrow 1$ ⚠	$0 \rightarrow 1 \rightarrow 0$ ⚠
$1 \rightarrow 0$	$1 \rightarrow 0$		$0 \rightarrow 1$	$1 \rightarrow 0 \rightarrow 1$ ⚠

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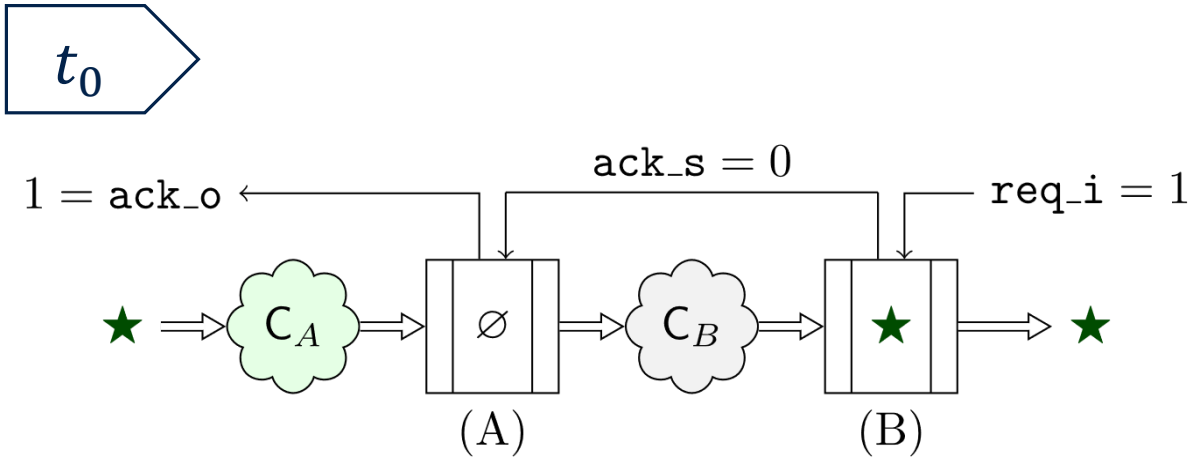
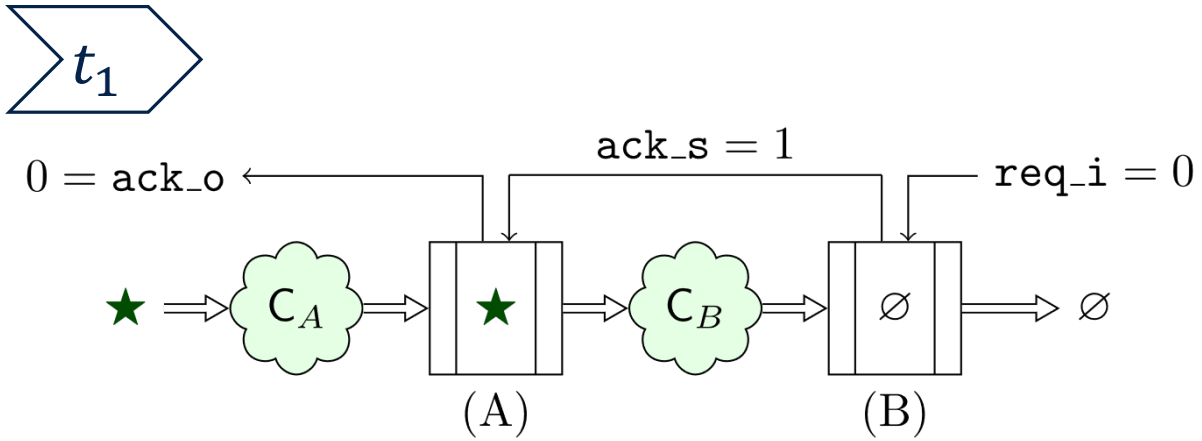
Avoiding Glitches

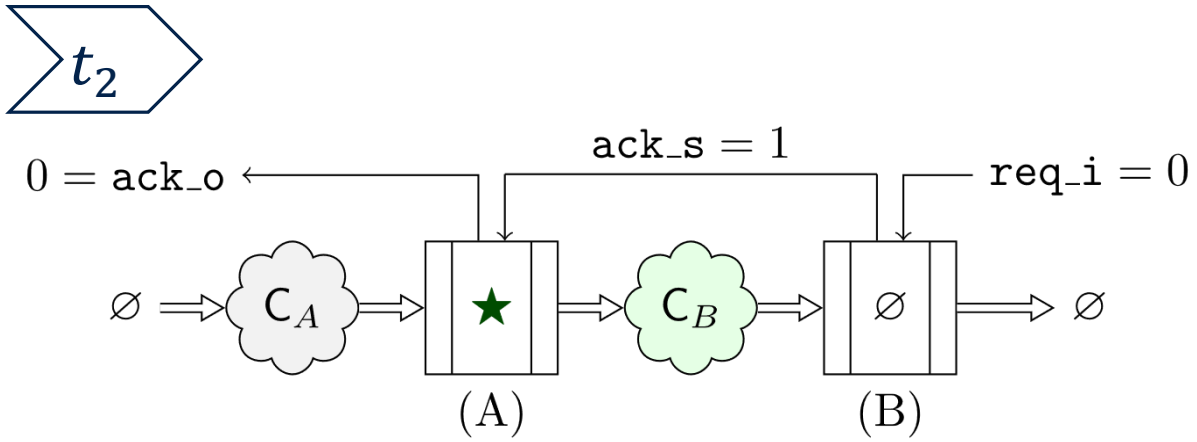
Pre-Charge Evaluate Logic + Monotonic Functions [PBM+20]

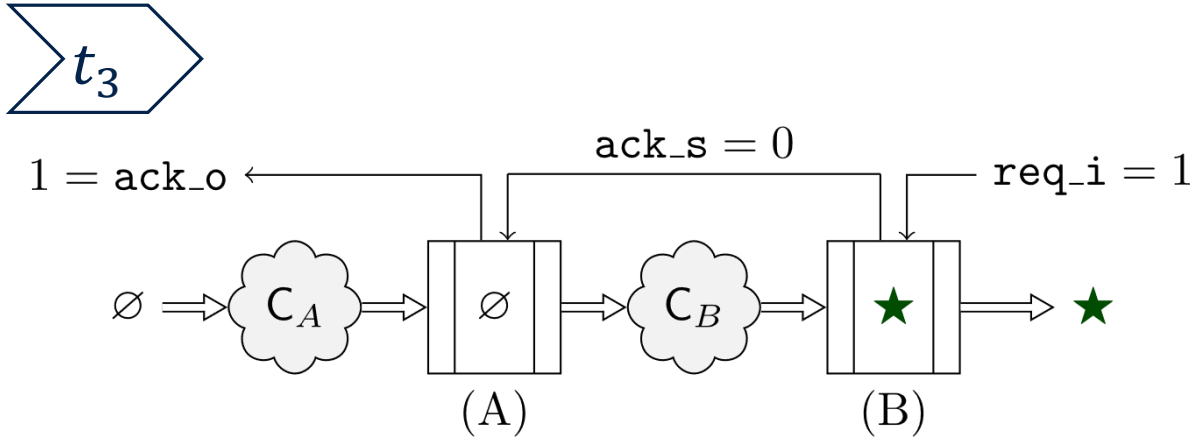
Stage	Input Transition		Dual-Rail Function	
	$a_I \rightarrow a_F$	$b_I \rightarrow b_F$	$z = a\ AND\ b$	$z = a\ XOR\ b$
Pre-charge	$0 \rightarrow \emptyset$	$0 \rightarrow \emptyset$	$0 \rightarrow \emptyset$	$0 \rightarrow \emptyset$
	$0 \rightarrow \emptyset$	$1 \rightarrow \emptyset$	$0 \rightarrow \emptyset$	$1 \rightarrow \emptyset$
	$1 \rightarrow \emptyset$	$0 \rightarrow \emptyset$	$0 \rightarrow \emptyset$	$1 \rightarrow \emptyset$
	$1 \rightarrow \emptyset$	$1 \rightarrow \emptyset$	$1 \rightarrow \emptyset$	$0 \rightarrow \emptyset$
Evaluate	$\emptyset \rightarrow 1$	$\emptyset \rightarrow 1$	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 0$
	$\emptyset \rightarrow 1$	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 1$
	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 1$	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 1$
	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 0$	$\emptyset \rightarrow 1$	$\emptyset \rightarrow 0$

Self-Timed Masking









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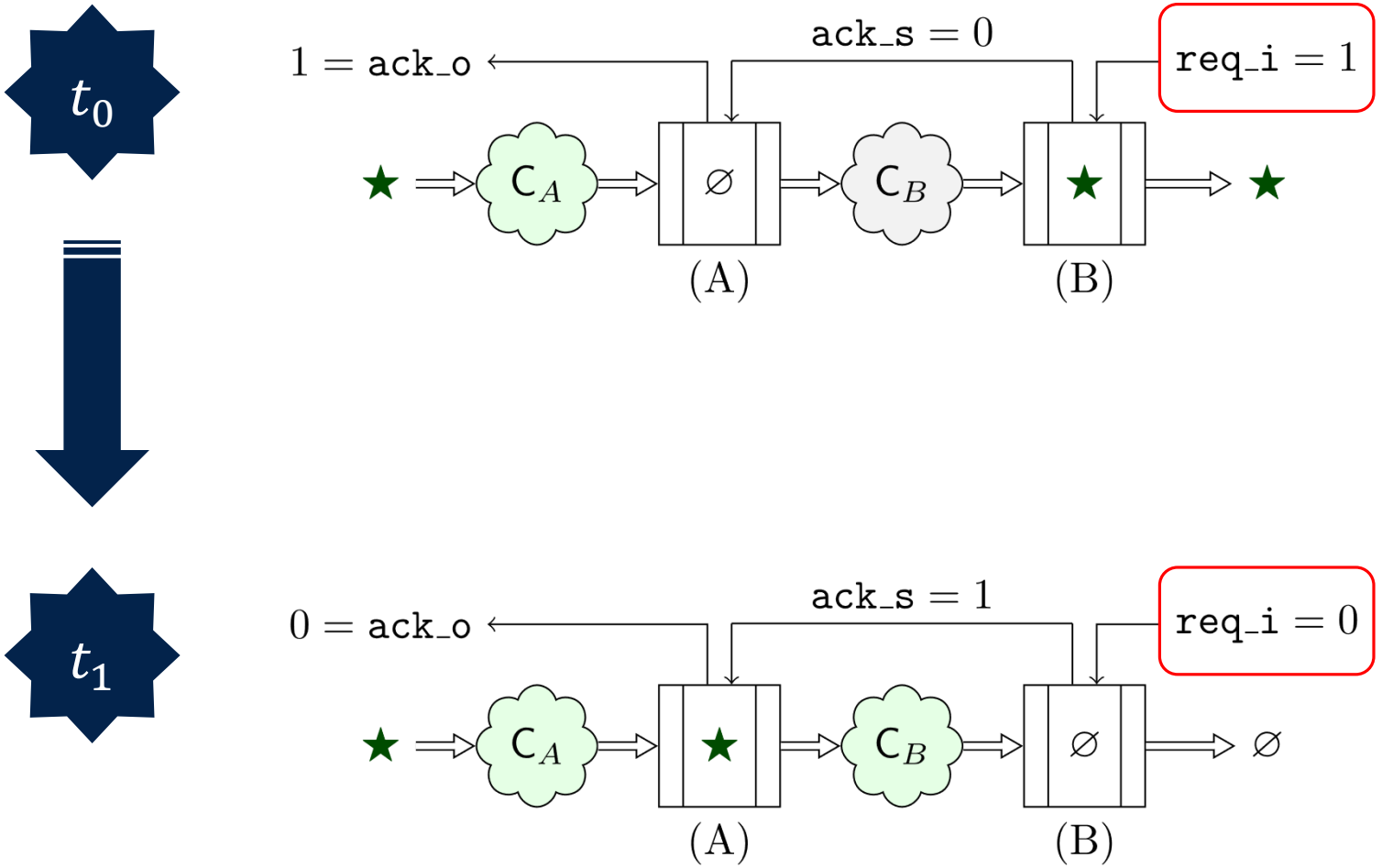
Self-Timed Masking



`req_i` paces the data flow in the pipeline

`ack_o` indicates the first latch state