Exploring the design possibilities of a PUF based on Ferroelectric Technology

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The promising features introduced by the integration of ferroelectricity into conventional transistor processes have led to extensive studies on device reliability, system-level applicability, and commercial viability. Its low-power characteristics make it particularly suitable for Internet of Things (IoT) applications, where a reliable power source cannot always be guaranteed. Additionally, its intrinsic memory properties make it a strong candidate for non-volatile memory implementations. Since these applications are data-intensive, the need to ensure secure data storage and transmission has motivated the adaptation of classic hardware security strategies to this emerging paradigm. Initially, researchers have explored the use of memory array operations to enable in-situ encrypted data storage [1]. Subsequently, the development of Nucleation Limited Switching (NLS) model introduced a level of stochastic behavior that has been leveraged for hardware-based Random Number Generators (RNGs), relying on the switching probability of ferroelectric domains [2]. In addition, numerous authors have demonstrated high robustness in PUF designs [3], exploring a range of models and strategies.

In this work, we aim to explore potential design approaches for implementing a PUF in ferroelectric technology, focusing on the variations expected in a commercial 28nm process and the exploitable stochasticity that arises when scaling down.

References

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