A Reliable 22nm Ferroelectric-based Non-Volatile SRAM Optimized for Critical Embedded Systems

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Ferroelectric-based non-volatile SRAMs (nvSRAM) are one of the most promising solutions that combines the fastest volatile memory (SRAM) and one of the most energy efficient emerging non-volatile memory (HZO-based ferroelectric capacitance, FeCAPs). An nvSRAM bitcell consists of an SRAM bitcell within which non-volatile BEOL ferroelectric capacitors (FeCAPs) have been integrated. This hybrid bitcell can then perform four different operations: (1) reading from SRAM (READ op.), (2) writing to SRAM (WRITE op.), (3) copying data from SRAM to FeCAPs (STORE op.) and (4) transferring data from FeCAPs to SRAM (RECALL op.). The resulting memory is thereby fast, energy efficient and non-volatile while being able to perform massive parallel STORE and RECALL ops. In this work, we use 6T4C nvSRAM bitcells [Fig. 1] in combination with a previously developed fast-erase mechanism [1] to (i) ensure fully functional RECALL even with SRAM ops. between STORE and RECALL, and (ii) counter cold-boot attacks while keeping data in the non-volatile part [Fig. 2].

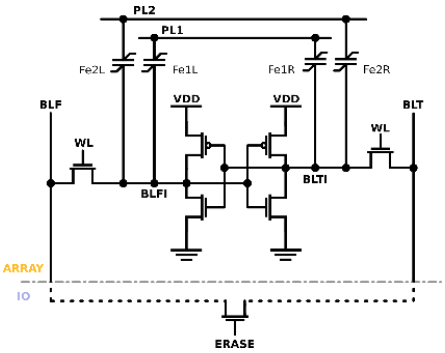

Fig 1. 6T4C nvSRAM bitcell with Fast-Erase

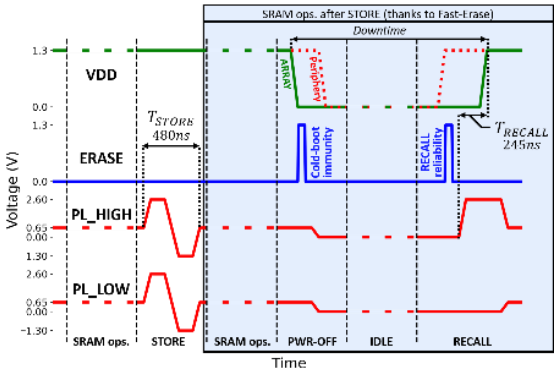

Fig 2. Operations chronogram

In a previous work [2], we demonstrated in simulations that reliable nvSRAM operations are achievable thanks to the fast-erase circuit and an optimized FeCAP sizing in a 130nm CMOS technology node. To go further, we now project these results on a 22nm CMOS technology node. All results come from SPICE simulations based on Monte-Carlo analyzes and a VerilogA model calibrated with silicon measurements on FeCAPs devices.

[1] J.-P. Noel et al., ''A Near-Instantaneous and Non-Invasive Erasure Design Technique to Protect Sensitive Data Stored in Secure SRAMs'', ESSCIRC, 2021
[2] L. Rhetat et al., "A Novel Design Technique for Enhanced Security and New Applications of Ferroelectric-Based Non-Volatile SRAM", VLSI-SOC, 2024